Heterogeneous Multi-Processor Pipelines: a Real-Time MPSoC Story

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Several modern systems, from ubiquitous mobile phones to powerful gaming machines, contain multiple heterogeneous processing cores. In a modern phone, for example, a general purpose processor manages the human machine interface, while a DSP manages the baseband signal processing. Usually, these heterogeneous multi-processor systems isolate tasks, and execute the isolated tasks in separate processors.

In this talk a novel heterogeneous multiprocessor pipeline system is described, where a single real-time streaming application is executed by multiple processors. The processors in the system are connected in a pipeline via queues (FIFOs) which allow communication at a higher bandwidth, devoid of the contention exhibited by typical shared bus architecture. Recent developments in Application Specific Instruction Set Processors (particularly from Tensilica Inc), have driven the creation of these multi processor pipelines with ASIPs as the building blocks. Each ASIP in the pipeline is customized with differing additional instructions, and instruction and data cache sizes to improve performance of the task mapped on that particular ASIP. As a result, the performance of the whole system is improved, while minimizing the increase in area. The permutation of configurations for each ASIP make up the design space of the pipelined multiprocessor system, and is rapidly explored. An automated design methodology to choose the best ASIP configurations as the final design in a reasonable amount of time is shown. The rapid exploration methodology used is able to explore design spaces up to $10^{16}$ design points, which is almost impossible to explore otherwise. Finally, the possibilities of merging pipeline systems are discussed.