Prediction of the impact of mutual inductance on timing towards nano-scale SoC

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Abstract—This paper suggests a method to predict the impact of mutual inductance (M) on interconnect signal delay estimation according to resistance (R), self-inductance (L), and capacitance (C) in nano-scale system on a chip (SoC). The proposed method first calculates the difference in delay between RLC and RLMC wire models for a set of parameter variations, then builds response surface functions (RSF) using physical parameters including wire width and spacing. The proposed method contributes to design rules to avoid mutual inductance effects.

I. INTRODUCTION

Impacts of on-chip inductance on signal propagation delay have been discussed [1]-[6] for 1 GHz or higher clock frequencies. The articles [1][2] revealed effects of on-chip self-inductance and then proposed methods for screening interconnects which should be treated as RLC models[7][8], rather than the conventional RC expressions[9]. As for the recent System-on-a-Chip (SoC) applications including 4K8K HDTV processing[10], processor cores need more speed to complete the required operations. Towards higher clock frequencies, the articles [3][4][5][6] pointed out necessity of taking into consideration the inductive coupling effects in timing analysis. In order to reappear the inductive coupling effects, we have to extract the mutual-inductance (M) in addition to the loop self-inductance (L)[11][12]. However, the existing papers have not explicitly suggested screening methods of on-chip mutual-inductance effects, which predict physical dimensions of interconnects to require RLMC models.

This paper proposes a method to screen the mutual inductance effects on timing in terms of physical dimensions including wire width, spacing, and distance from the aggressor. It reveals layout pattern dependence of the RLC delay estimation error. Using the proposed method, we can minimize signal delay estimation errors associated with the inductive coupling.

II. SCREENING METHOD OF THE IMPACT OF MUTUAL INDUCTANCE ON TIMING

The overall flow consists of the following two steps.

A. Estimating difference in signal propagation delay between wire models with and without mutual inductance (M).

B. Generating RSF to predict the delay difference between RLMC and RLC models using physical dimension for mutual inductance impact evaluation along with precise timing analysis.

A. Estimation of difference in signal propagation delays

Three dimensional interconnect structures under test have cross-sectional dimensions including metal and dielectric thickness defined by the wafer process technologies. Conversely, horizontal dimensions such as width, spacing, and length of wires can be managed by designers. The horizontal dimension parameters are treated as variables. Figure 1 shows the interconnect structure. We assume regular meshes of ground grids that provides the return current. Here, all neighbors are considered as candidates of the current return path during RLC extraction with the lumped self-inductance $L$. On the other hand, selection of the current return path affects inductive coupling effects between the objective (victim) and the aggressor wires. To avoid excessive pessimism, the substrate plane is treated as the current return path when extracting RLMC. The extracted RLC and RLMC form ladders so that the unit length is sufficiently small compared to the wave length derived by the significant frequency $f_s$, $f_r$, and $f_f$. It is expressed as the function of the signal rising time $t_r$ and the signal falling time (Eq.(1)). The driver size is determined so that the transition at the receiver becomes $t_r$ and $t_f$.

$$f_s = \max \left( \frac{0.35}{t_r}, \frac{0.35}{t_f} \right)$$  \hspace{1cm} (1)
TABLE I : Predictor variables $x_i$ to predict the difference between RLMC and RLC delays.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{min}/S$</td>
<td>Reciprocal of wire spacing normalized by the minimum.</td>
</tr>
<tr>
<td>$W/W_{min}$</td>
<td>Wire width normalized by the minimum.</td>
</tr>
<tr>
<td>$l/l_{min}$</td>
<td>Wire length normalized by the minimum.</td>
</tr>
<tr>
<td>$D_{min}/D$</td>
<td>Reciprocal of distance from the aggressor norm. by the pitch.</td>
</tr>
</tbody>
</table>

TABLE II : Interconnect parameter and constant for 14nm node.

<table>
<thead>
<tr>
<th>Parameter, Constant</th>
<th>Unit</th>
<th>Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative diel. const.</td>
<td>-</td>
<td>2.375</td>
</tr>
<tr>
<td>Wire sheet resistance</td>
<td>Ω/□</td>
<td>5.08</td>
</tr>
<tr>
<td>Wire thickness $t$</td>
<td>nm</td>
<td>89</td>
</tr>
<tr>
<td>Wire height $h$</td>
<td>nm</td>
<td>1015.8</td>
</tr>
<tr>
<td>Wire spacing $S$</td>
<td>$S_{min} = 190nm$</td>
<td>$\times 1, 2, 4, 8, 16$</td>
</tr>
<tr>
<td>Wire width $W$</td>
<td>$W_{min} = 190nm$</td>
<td>$\times 1, 2, 4, 8, 16$</td>
</tr>
<tr>
<td>Wire length $l$</td>
<td>$l_{min} = 10\mu$m</td>
<td>$\times 1, 2, 4, 8, 16$</td>
</tr>
<tr>
<td>Distance from aggressor</td>
<td>$Pitch = W + S$</td>
<td>$\times 1, 2, 3$</td>
</tr>
</tbody>
</table>

B. Response surface function generation

After differences between RLC and RLMC delays are estimated for the parameter variation, the screening equations are built using response surface methods (RSM)[13]. We build response surface functions (RSF) expressed as Eq.(2), based on the physical dimension parameters. $f()$ stands for fourth order polynomials separated by cases where the aggressor and the victim transition in the same (even), and the opposite (odd) directions.

$$RSF = f(x_1, x_2, \ldots, x_i, \ldots, x_n) + \epsilon$$ (2)

In Eq.(2), $x_i$ denotes predictor variables which predicts the difference between RLMC and RLC delays, and $\epsilon$ expresses residual error in the prediction. In detail, referring the amount of mutual inductance[11][12] as well as the relative ratio of reactance[14], we define the RSF as the fourth order polynomial functions of the predictor variables shown in Table I.

It can contribute to estimate the inductance impact in floorplanning, or physical design phases.

III. Quantitative Evaluation of the Screening Method in a 14nm FinFET Process

Based on the parameters in International Technology Roadmap for Semiconductors (ITRS) [15] along with Predictive Technology Model (PTM)[16], the interconnect structure with buffers and receivers for high-performance SoC are defined as shown in Table II.

IV. Conclusion

We apply the proposed method to the 14 nm technology node to evaluate prediction of the mutual inductance effects. Size of the drivers and the receivers is x64 of the unit size[17] so that $t_i$ and $t_j$ becomes 10ps., where the operating frequency is targeted at 10GHz and the significant frequency $f_i$ is 35GHz. The corresponding wavelength is 3.6mm. According to a preliminary experiment, domain of the horizontal dimension parameters are decided so that the maximum delay difference exceeds 3%. Since the wire length is below a quarter of the wavelength, we apply a FEM based 2.5D field solver[18]. Figure 2 compares RLC and RLMC waveforms. Figure 3 shows the RLC delay estimation errors compared to the RLMC delays with the corresponding predictions using the RSFs. The degree of freedom adjusted coefficient of determination ($R^2$) exceeds 0.9, which indicates that the prediction has good fit[13]. Figure 4 shows an impact dependency on distance from the aggressor.

This paper suggested a methodology to precisely predict and screen the impact of mutual inductance on interconnect signal delay estimation in a nano-scale system on a chip (SoC). The proposed methodology first calculates the delay difference between $RLC$ and $RLMC$ wire models for a set of parameter variations, then builds RSFs using physical parameters including wire width and spacing. The proposed methodology can help to define design rules for avoiding mutual inductance effects as well as to point out wires that require $RLMC$ delay calculation.
Fig. 3: Prediction accuracy of the delay estimation without mutual inductance.

Fig. 4: Predicted impact dependency on distance from the aggressor. (L:×16, W:×16, S:×1)

REFERENCES


