Precise Expression of nm CMOS Variability with Variance/Covariance Statistics on Ids(Vgs)

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Abstract - Choice of Compact MOS models and determination of their parameters are of primary importance to achieve high quality mixed signal SOC design. In nm-CMOS, the critical issue is how to precisely express performance variability in SPICE model parameters including geometry (gate area) and bias dependent fashion. On the MOS geometry dependence, Pelgrom's formulation is known to be reasonably accurate in using Compact MOS models. However, reflecting the bias dependent variation on the SPICE parameters stays in research level. We have measured the drain current (Ids) variation of various sized CMOS under different gate bias conditions (Vgs). Both variation sigma (standard deviation) of Ids and correlations among Ids, Vth and Gm are considered to play important role in accurate expression of the device/circuit performance variations especially for analog circuits. This paper provides accurate model parameter extraction methodology considering such size and bias dependence of the sigma and the correlations.

I. Introduction

Compact MOS model is basically excellent mixture of physical and practical mathematical formulations. Therefore, various optimization algorithms have been developed to extract its parameters based on error minimization between experiments and model calculation results [1, 2]. In this context, it is very important how to define error which reflects real application in circuit simulations [3]. In nm-CMOS, random variability of CMOS performance has been increased drastically, and then it becomes one of the challenging issues how to formulate the variability on the model parameters and how to extract parameter variabilities from experimental data. K. Takeuchi et al. showed statistical parameter extraction scheme combined with PCA (Principal Component Analysis) technique [4, 5]. C. C. MacAndrew et al. proposed sensitivity-based variability parameter extraction approach called BPV (Backward Propagation of Variation) method [6, 7]. It is an optimization approach to minimize error of statistical variation sigma (standard deviation) on drain current σ(Ids) based on sensitivities of the Ids versus model parameters. However, it focuses only on the variation sigma of model parameters and neglects statistical correlation between them, also neglects correlation among drain current performances, such as the correlation between threshold voltage (Vth) and on-current (Ion) [8]. B. Cheng et al. also reported a statistical compact modelling strategy based on an "atomic" device simulation [9]. In the paper, extracted statistical model parameters reproduced well the simulated Ids and Vth variations as well as their correlation data. However, the work has been done for single geometry MOS transistor under the fixed on-current bias condition.

In this paper, we propose a new method to determine model-parameter variabilities. It allows accurate bias-dependent statistical modelling with excellent agreement with experimental variations (both of variance and covariance) in device model used in circuit simulation. In addition we have also developed geometry dependent formula for the variability parameters to allow using it in analog circuit designs.

II. Variability Measurement Results

A. Geometry effects

In nm-devices, random dopant fluctuation (RDF) plays an important role in variability of CMOS drain current. The effects of the RDF are in proportion with inverse of square root of gate area [10]. Figure 1 and 2 show typical experimental data that demonstrate the relation for NMOS and PMOS, respectively. Sample size of the measurement is 72 (chips) each for 13 different gate area devices. As demonstrated in the figures, the linear relationship between the on current variation and a gate area function is good enough approximation in using compact MOS model application. It is noted that the slope found in the figures is investigated in detail in [11], however, the linear relation is still valid even in smaller-sized CMOS.

B. Bias effects

Figure 3 depicts a typical set of Gm-Vgs curves measured with identical NMOS located on a same chip. It is well demonstrated the RDF (Random dopant Fluctuation) affects [10] on the drain current characteristics. We focus measurement of the drain current variation with gate bias (Vgs) dependent fashion.

Figure 4 is a measurement result showing Vgs dependency of relative drain current variation. Vertical axis indicates drain current variation sigma (standard deviation) divided by average drain current. As shown in the figure, the value monotonically reduced as the Vgs increases. Note that the data biased below the NMOS threshold voltage (Vth) are not reliable because of measurement limit below nano-ampear range. The monotonic decrease of the variability can be roughly interpreted due to the Vth variation caused by

RDF. This is because the effective gate bias (Vgs-Vth) variation is reduced as the gate bias is increased.

Figure 5 shows gate bias effect on transconductance (gm) variation on the same devices. This data is very important in analog circuits design. Important indication of the data is that the gm variation shows maximum value at around Vg=0.6V. The gate bias is usually used as DC bias point in most of analog circuits such as operational amplifiers.

C. Correlations

Statistical nature of variation is composed of not only variation sigma but also correlation characteristics between physical quantities. If the drain current variation is caused only by the threshold voltage variation, correlation coefficient between the two should be one (full correlation). However measurement says it is not. Figure 6 shows Ion-Vth scatter plot, here the Ion is drain current at Vgs=Vdd (1.0V). The experiment shows relatively weak correlation between the Vth and Ion. It means other variation sources will exist except the Vth variation (RDF), such as carrier mobility or gate oxide local fluctuation etc. Figure 7 shows gm-Vth correlation at Vgs=Vdd bias condition. The result exhibits very low correlation between the two. Gate bias dependences of the correlation coefficients for Ion-Vth and gm-Vth characteristics are given in Figure 8.

It is noted that these experimental data of variation sigma and these statistical correlation between device parameters have to be correctly reflected on circuit simulation with their bias dependence.

III. Variability Parameter Extraction

A. Extraction algorithm

BSIM4 [12] was selected as an example target compact MOS model for the variability parameter extraction. Firstly we have chosen VTH0 and TOXP as variability parameters to express drain current variation. Assume measurement data of variabilities of Ids-Vgs, gm-Vgs, and Vth for NMOS and PMOS with various geometries (L & W) are available. These data are used to extract statistical quantities of variability parameters *VTH0* and *TOXP*. The statistical quantities mean the variation sigma of the two model parameters and the correlation coefficient between them.

Measured Vth and Ids variation can be statistically formulated as follows:

$$\Delta V_{th} = \frac{\partial V_{th}}{\partial VTH0}\Delta VTH0 + \frac{\partial V_{th}}{\partial TOXP}\Delta TOXP, \quad (1)$$

$$\Delta I_{on} = \frac{\partial I_{on}}{\partial VTH0}\Delta VTH0 + \frac{\partial I_{on}}{\partial TOXP}\Delta TOXP, \quad (2)$$

where $S_{i,j}$ are the sensitivities defined as follows.

$$S_{11} = \frac{\partial V_{th}}{\partial VTH0} \quad (3)$$

$$S_{12} = \frac{\partial V_{th}}{\partial TOXP} \quad (4)$$

$$S_{21} = \frac{\partial I_{on}}{\partial VTH0} \quad (5)$$

$$S_{22} = \frac{\partial I_{on}}{\partial TOXP} \quad (6)$$

Assuming the random variables follow normal distributions with mutual correlation, statistical expression of the above equations are transformed into the following,

$$Var(V_{th}) = S_{11}Var(VTH0) + S_{12}Var(TOXP) + 2S_{11}S_{12}Cov(VTH0, TOXP) \quad (7)$$

$$Var(I_{on}) = S_{21}Var(VTH0) + S_{22}Var(TOXP) + 2S_{21}S_{22}Cov(VTH0, TOXP) \quad (8)$$

where $Var(p)$ denotes variance of p and is equal to $\{\sigma(p)\}^2$, and $Cov(p,q)$ denotes covariance between p and q, and equals to $\sigma(p)\sigma(q)\rho(p,q)$. According to the properties of covariance, the following equation holds.

$$\begin{aligned} Cov(V_{th}, I_{on}) &= S_{11}S_{21}Cov(VTH0, VTH0) \\ &+ S_{12}S_{22}Cov(TOXP, TOXP) \\ &+ S_{11}S_{22}Cov(VTH0, TOXP) \\ &+ S_{12}S_{21}Cov(TOXP, VTH0) \end{aligned} \quad (9)$$

Equations (7), (8), (9) can be rewritten to the following one simultaneous:

$$\begin{pmatrix} S_{11}^2 & S_{12}^2 & 2S_{11}S_{12} \\ S_{21}^2 & S_{22} & 2S_{21}S_{22} \\ S_{11}S_{21} & S_{12}S_{22} & S_{11}S_{22} + S_{12}S_{21} \end{pmatrix} \begin{pmatrix} Var(VTH0) \\ Var(TOXP) \\ Cov(VTH0, TOXP) \end{pmatrix} = \begin{pmatrix} Var(V_{th}) \\ Var(I_{on}) \\ Cov(V_{th}, I_{on}) \end{pmatrix} \quad (10)$$

where $Var(VTH0)$, $Var(TOXP)$ and $Cov(VTH0, TOXP)$ are unknowns.

The overall extraction process is as follows.

1. Measure $Var(V_{th})$, $Var(I_{on})$ and $Cov(V_{th},I_{on})$
2. Calculate sensitivities S_{ij} using SPICE with the nominal model parameters
3. Solve Eq. (10) and get $\sigma(VTH0)$, $\sigma(TOXP)$, $\rho(VTH0, TOXP)$

B. Geometry modelling

By using the statistical form, we have extracted variability parameters for NMOS and PMOS with various geometries. However the data obtained from the series of extraction works are dotted data of MOS geometrical sizes. Therefore we need to smoothly connect them by a simple mathematical geometry model (scaling the parameters) to enable circuit simulations including arbitrary sized transistors.

Scaling equation we used in this study is as follows;

$$P = P_0 + \frac{P_1}{\sqrt{LW}} + \frac{P_2}{L} + \frac{P_3}{W} \quad (11)$$

The above equation is an empirical one, however, the second term comes from Pelgrom's area dependent formula [10] and the third/fourth terms imply peripheral length dependency. Note that the parameters P_1, P_2 and P_3 have the same physical dimension.

C. Results

Firstly we evaluated very simple example in which only $\sigma(V_{th})$ is the fitting target and only $\sigma(VTH0)$ is extracted. Figure 9 shows the extracted result demonstrated as V_{th}-I_{on} scatter plot for NMOS with L=0.13μm and W=0.18μm. Because the correlation between V_{th} and I_{on} is neglected in

the extraction, the experimental agreement is poor as expected.

Next, the proposed variability parameter extraction has been conducted on the same device and the result is shown in Figure 10. In this example, two variability parameters are chosen; VTH0 and TOXP in BSIM4 model parameters. The $\sigma(V_{th})$, $\sigma(I_{on})$ and correlation coefficient $\rho(V_{th}, I_{on})$ are the target quantities for variability parameter extraction. As shown in the figure, measured and simulated correlations between V_{th} and I_{on} match reasonably well. Gate bias dependences of σ(Id) and ρ(Vth, Ion) are compared in Figure 11. The comparison shows that our variability parameter extraction is effective, and the gate bias dependence can better be expressed by increasing the number of statistical parameters extracted.

To demonstrate the feasibility of the scaling method using equation (7), directly extracted values of $\sigma(VTH0)$, $\sigma(TOXP)$, $\rho(VTH0, TOXP)$ are compared with their scaled value using equation (7), and depicted in Figure 13. P0, P1, P2, P3 are determined using least square method.

It shows that the scaling is successful for both standard deviation and correlation coefficient.

IV. Conclusion

We have measured the drain current (Ids) variation for various sized CMOS under various gate bias conditions (Vgs). Both variation sigma of Ids and correlations among Ids, Vth and Gm depend on the gate bias. These dependences can play an important role in accurate expression of the device/circuit performance variations especially for analog circuits. This paper provides accurate statistical model parameter extraction methodology for compact MOS models. The methodology takes the bias dependence into consideration, and also provides the scaling method which allows the extracted statistical parameters to be applied to various sized transistors.

References

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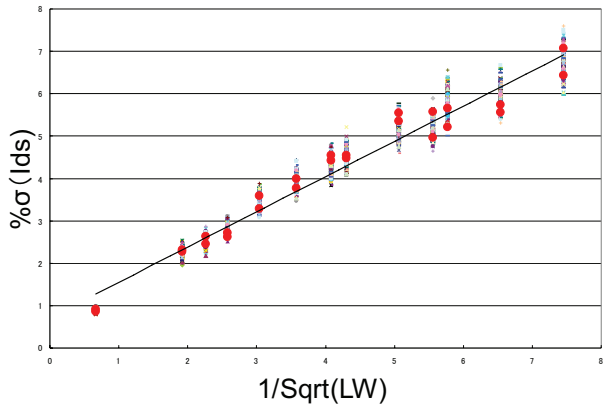


Fig. 1 Typical experimental data of Pelgrom's plot for NMOS Ids.

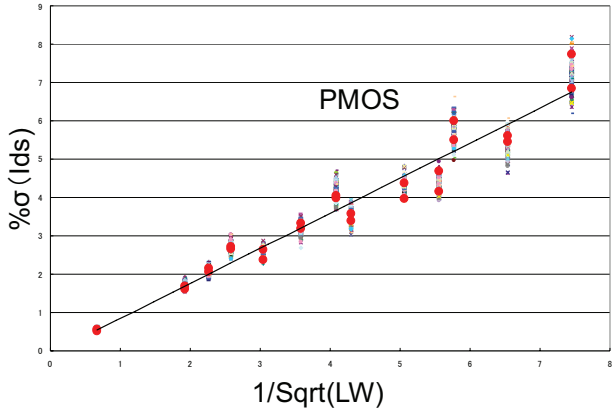


Fig. 2 Typical experimental data of Pelgrom's plot for PMOS Ids.

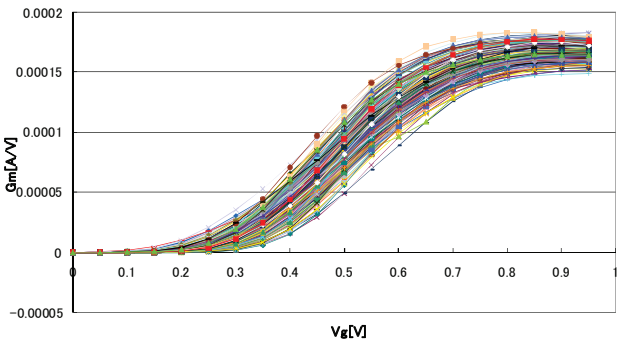


Fig. 3 Typical set of gm-Vgs curves measured with identical NMOS located on a same chip.

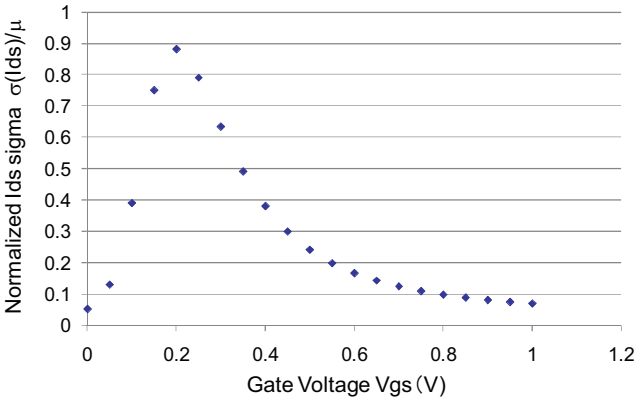


Fig. 4 Measurement result showing Vgs dependency of relative drain current variation.

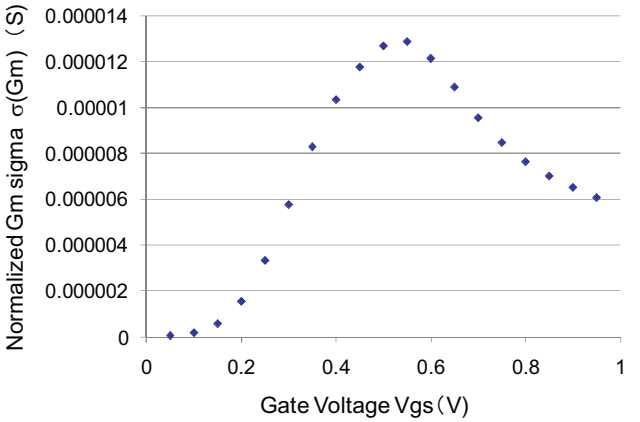


Fig. 5 Gate bias effect on transconductance (gm) variation on the same devices.

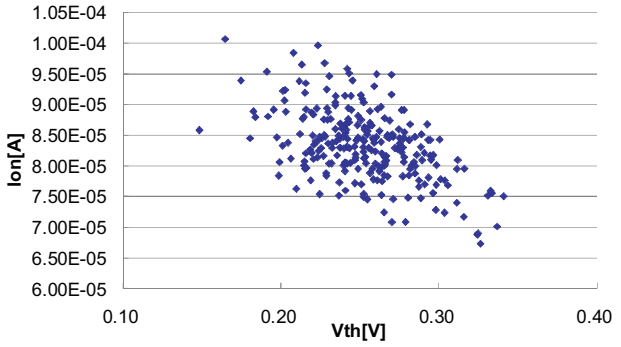


Fig. 6 Ion-Vth scatter plot, here the Ion is drain current at Vgs=Vdd (1.0V).

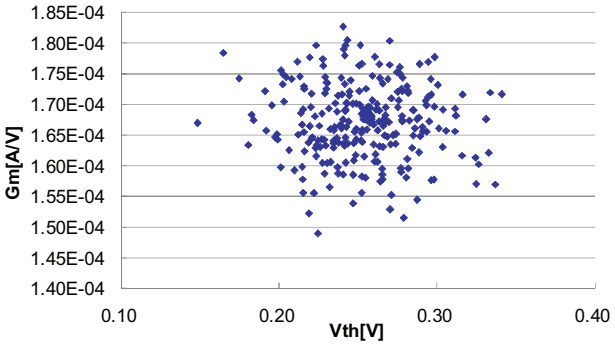
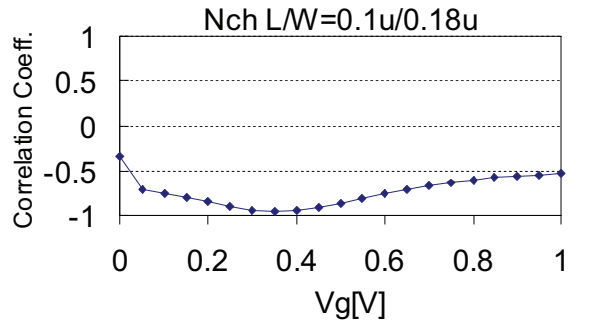
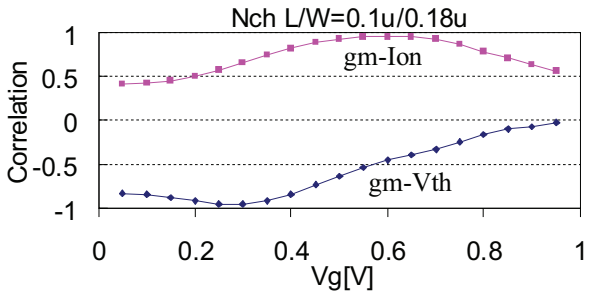


Fig. 7 The gm-Vth correlation plot at Vgs=Vdd bias condition.



(a) Ion-Vth correlation



(b) gm-Vth and gm-Ion correlation

Fig. 8 Gate bias dependences of the correlation coefficients for (a) Ion-Vth and (b) gm-Vth characteristics.

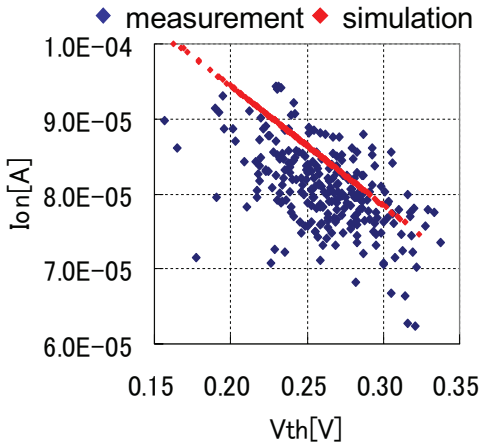


Fig. 9 "One variability-parameter" (VTH0) extraction; the result demonstrated on Vth-Ion scatter plot for NMOS with L=0.13um and W=0.18um.

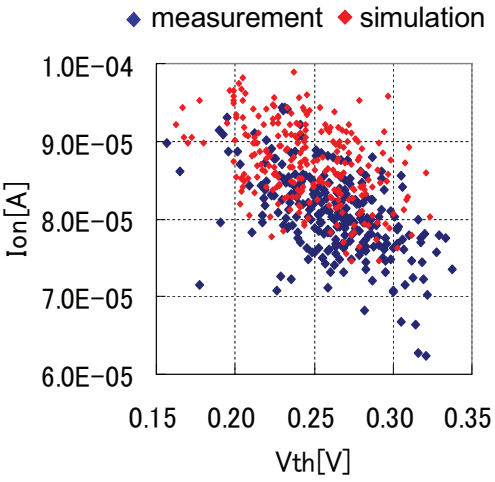
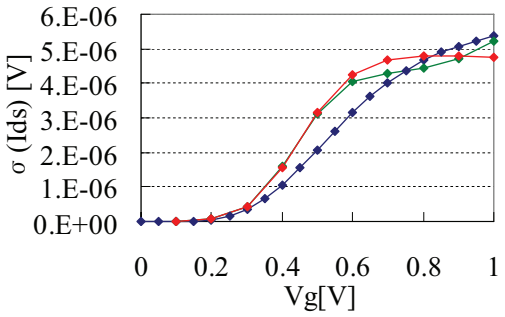
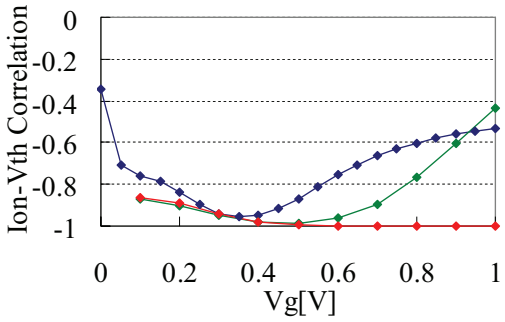


Fig. 10 Proposed "two variability-parameters" extraction on the same device shown in Figure 9.

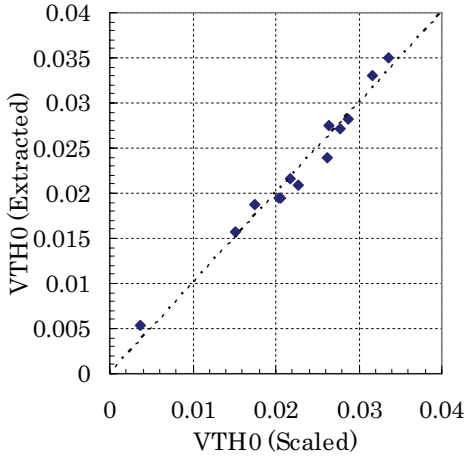


(a) $\sigma(I_{ds})$

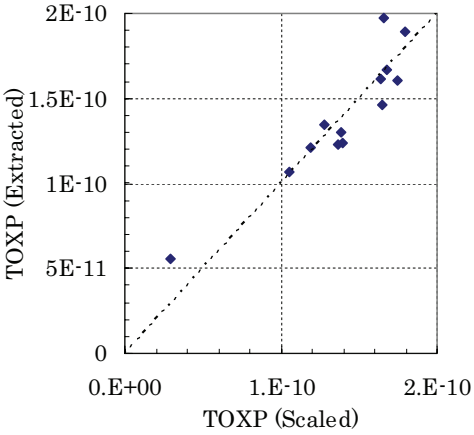


(b) $\rho(V_{th}, I_{on})$

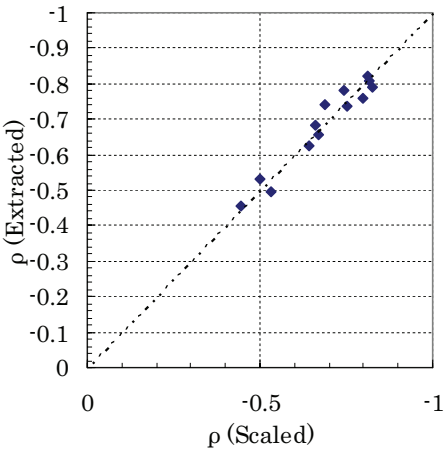
Fig. 11 Comparison of gate bias dependence
NMOS with L=0.1um, W=0.18um
blue: measured,
red: one parameter (VTH0) extraction,
green: two parameter (VTH0, TOXP) extraction



(a) $\sigma(VTH0)$



(b) $\sigma(TOXP)$



(c) $\rho(VTH0, TOXP)$

Fig. 12 Comparison of extracted value and scaled value for NMOS with sizes L/W=0.1/0.18, 0.1/0.3, 0.1/0.6, 0.1/0.15, 0.13/0.18, 0.13/0.3, 0.13/0.6, 0.13/1.5, 0.18/0.18, 0.18/0.3, 0.18/0.6, 0.18/1.5, 1.5/1.5 (unit is um)