Resistivity-based Modeling of Substrate Non-uniformity for Resistance Extraction of Low-Resistivity Substrate

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ABSTRACT

This paper discusses modeling of non-uniform substrate resistivity for substrate resistance extraction. Though substrate resistivity of each substrate layer is frequently assumed to be uniform, doping profile of each substrate layer is not uniform. We present the extraction error of substrate resistance under uniform resistivity assumption. The resistivity models we suggest enable accurate resistance extraction of substrate with non-uniform profile. We also demonstrate characterization of the suggested model using substrate resistances which are easily obtained from fabricated chips.

I. INTRODUCTION

Substrate noise is commonly known as one of the factors which deteriorate performance of analog circuits on LSI. Accurate estimation of substrate noise is required for circuit design to reduce the impact of substrate noise and to minimize the area overhead due to noise immunity design. There are many reports about substrate noise, such as measurements of substrate noise on the fabricated chip [1–4], extraction methods of substrate resistance [5–7], simulation methods of substrate noise [2, 3, 8–11], and modeling of noise source for fast simulation of substrate noise [4].

For extraction of substrate resistance, past works frequently adopted an assumption that resistivity of each substrate layer (surface layer, epi-layer, high-resistivity layer, and so on) is uniform [5, 6]. However, the adequacy of the assumption of uniform resistivity or the extraction error due to the assumption has been scarcely discussed. Though several past works [10, 11] apply doping profile of the process for substrate extraction, discussions about the uniform resistivity assumption cannot be found.

This paper discusses non-uniformity of the substrate resistivity. The contributions of this paper are as follows.
1) Revealing that non-uniformity of substrate resistivity causes considerable error in substrate resistance extraction.
2) Suggesting substrate resistivity models which solve extraction problem due to non-uniformity of substrate resistivity.
3) Demonstrating the characterization of the suggested model with substrate resistance which can be easily obtained from fabricated chips.
Section II. describes the assumption that resistivity of each substrate layer is uniform and non-uniformity of substrate resistivity. In Sec. III.A., we demonstrate that under uniform resistivity assumption, extracted substrate resistance includes considerable error in comparison with resistance extraction results with substrate impurity doping profile. Sec. III.B. suggests a stepwise resistivity model and an interpolation model for substrate resistance extraction considering non-uniform resistivity of substrate. Extraction errors with uniform resistivity model were notably reduced by suggested models. Evaluation in Sec. IV. demonstrates the characterization of interpolation model with substrate resistance which can be easily obtained from fabricated chips.

II. UNIFORM RESISTIVITY ASSUMPTION AND DOPING PROFILE OF SUBSTRATE

Figure 1 shows typical structures of high-resistivity and low-resistivity substrates [12]. High-resistivity substrate has a low-resistivity layer on a high-resistivity bulk. The bottom of low-resistivity substrate has low-resistivity, and a high-resistivity layer is inserted between the bottom layer and the surface layer. Resistivities of each layer of high-resistivity and low-resistivity layers are frequently assumed to be uniform in past works [5, 6].

On the other hand, impurity doping profile of each substrate layer is not uniform. Thermal diffusion and ion implantation are representative methods of impurity doping, and are used in a complementary style. For example, thermal diffusion is adopted for deep substrate layers such as a twin-well structure, and ion implantation is applied for source/drain area of MOS. 'Predeposition' and 'drive-in' are two major ways of thermal diffusion Predeposition is carried to the surface of substrate to be doped by diffusion. The impurity deposited on the surface is diffused by 'drive-in', and a deep junction can be formed. The impurity distribution after 'drive-in' is given by:

$$C(x) = C_s \cdot (1 - \frac{2}{\pi} \int_0^{x/2\sqrt{(DT)}} e^{-y^2} dy) \qquad (1)$$

where x is the distance into substrate, $C(x)$ is impurity concentration at distance x, C_s is impurity concentration at the

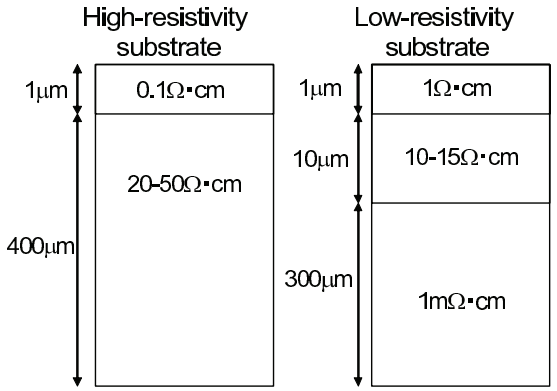


Fig. 1. Structure of high-resistivity and low-resistivity substrate [13].

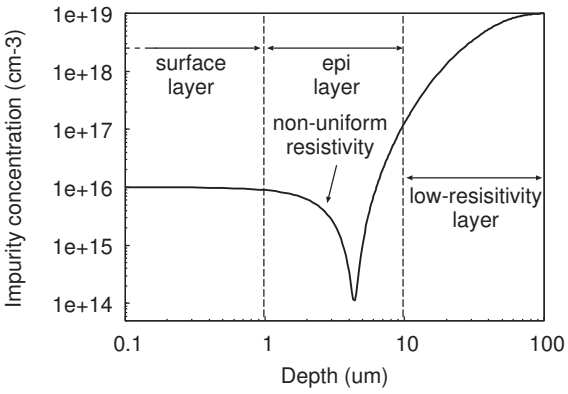


Fig. 2. An example of impurity concentration profile based on the low-resistivity substrate of Fig. 1. Average resistivities of surface layer, high-resistivity layer, low-resistivity layer are 1.5Ω·cm, 9.2Ω·cm, and 17mΩ·cm respectively.

surface, D is the diffusion coefficient, and T is the diffusion time [13]. Figure 2 shows a sample of the doping profile when low-resistivity substrate of Fig 1 was assumed to be formed with thermal diffusion. We assumed that boron and phosphorus are respectively doped once into the substrate which had $10^{19}/cm^3$ p-type uniform impurity concentration. The resistivities of the surface layer, the epi-layer, and the low-resistivity layer are $1.6\Omega{\cdot}cm$, $9.2\Omega{\cdot}cm$, and $17.2\text{m}\Omega{\cdot}cm$. Though resistivity of each layer is almost equal to the resistivity in Fig. 1, epi-layer has non-uniform resistivity which varies from 2 to $120\Omega{\cdot}cm$, which can be calculated from resistivity of p-type (boron doped) substrate.

III. Modeling of substrate resistivity

This section demonstrates the extraction error of substrate resistance when each substrate layer is modeled with uniform resistivity assumption. The current distribution in the substrate which causes extraction error is discussed and layout patterns where error is observed are explained. We also suggest the substrate resistivity models which improve these errors. These models provide the approximation of substrate resistivity profile.

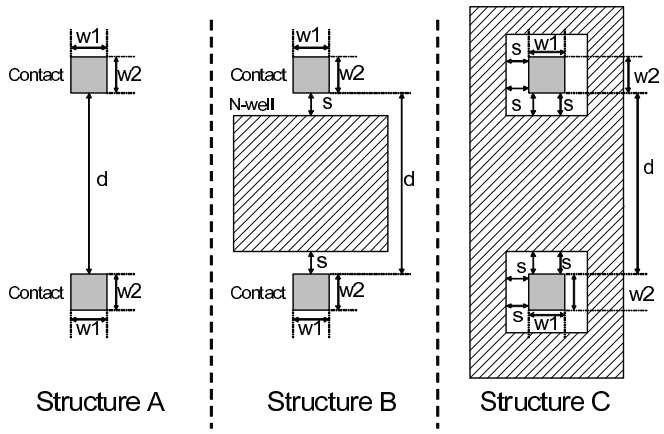


Fig. 3. Test structures.

A. Extraction error under uniform resistivity assumption

This section demonstrates substrate resistance when the substrate is modeled with uniform resistivity for each substrate layer and doping profile. Figure 3 depicts the layouts for resistance extraction, and parameters of the layouts are shown in Tab. I. LAYOUT.1 is a simple two-contact structure. N-well is placed nearby the each contact in LAYOUT.2-4. Each contact is larger than LAYOUT.1 in LAYOUT.5. LAYOUT.6 includes two adjacent contacts. Substrate resistance between two contacts is extracted for each layout by substrate resistance extraction tool [14].

Table II shows the extraction results of substrate resistance. We assumed two doping profiles of an industrial low-resistivity substrate process and Fig. 2 profile. Depth of N-well is assumed to be 4μm in Fig. 2 profile. The technology information of the industrial process is confidential, and the dimensions of layouts are slightly changed for the resistance extraction with the industrial process. Table II also includes extraction results when resistivity of each substrate layer is assumed to be uniform (uniform resistivity assumption). Doping profile can be confirmed in Fig. 2 profile though the doping profile of the industrial process is confidential. Adequacy of extraction results with Fig. 2 profile is validated by the extraction results with the industrial process. We can observe the increase of resistance in the case that contacts are close to N-well (LAYOUT.3,4) from extraction results of doping profile. On the other hand, substrate resistance decreases when the two contacts are close or large. We can find extraction errors in these layout patterns under the uniform resistivity assumption, and extraction errors of the industrial process and Fig. 2 show similar tendency.

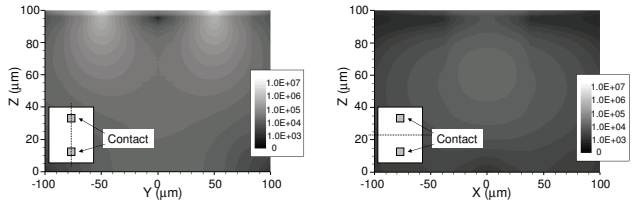
These errors are caused by the inaccurate estimation of current distribution. Figures 4 and 5 show the cross-sectional views of the substrate current distribution extracted with a 3D

TABLE I
TEST PATTERNS

No.	structure	w1(μm)	w2(μm)	d(μm)	s(μm)
LAYOUT.1	A	5	1	100	-
LAYOUT.2	B	5	1	100	10
LAYOUT.3	B	5	1	100	1
LAYOUT.4	C	5	1	100	1
LAYOUT.5	A	10	10	100	-
LAYOUT.6	A	5	1	2	-

TABLE II
SUBSTRATE RESISTANCE EXTRACTION RESULTS. SUBSTRATE MODELS WITH DOPING PROFILE AND UNIFORM RESISTIVITY ARE COMPARED.

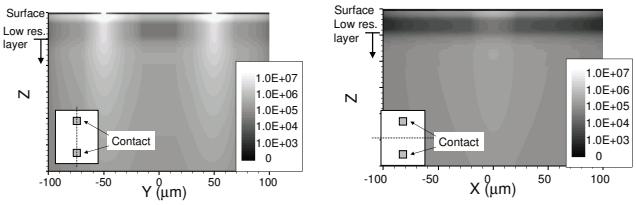
	Fig. 2 profile		Industrial process	
No.	Detailed profile (Ω)	Uniform res. (Ω)	Detailed profile (Ω)	Uniform res. (Ω)
LAYOUT.1	12771	13234	1242	1169
LAYOUT.2	13163	13294	1313	1192
LAYOUT.3	15822	13336	1380	1060
LAYOUT.4	81433	17664	7042	1258
LAYOUT.5	4027	2379	669	353
LAYOUT.6	6049	9157	531	913



(a) Cross-section along two contacts

(b) Cross-section between two contacts

Fig. 4. Current density (A/m^2) of substrate cross section with Fig 2 profile.

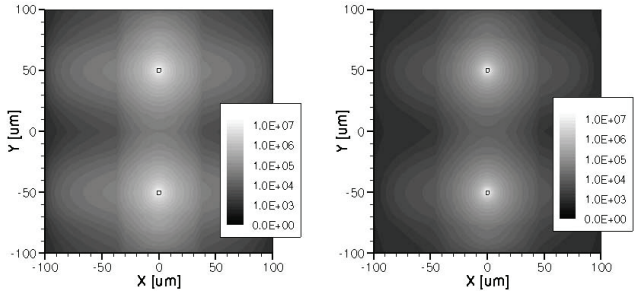


(a) Cross-section along two-contacts

(b) Cross-section between two contacts

Fig. 5. Current density (A/m^2) of substrate cross section with an industrial process of low-resistivity substrate.

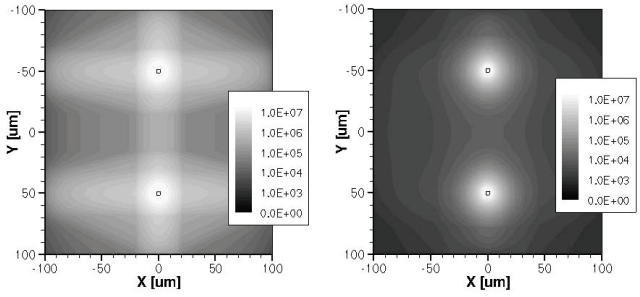
field solver [15]. Two contacts are placed on the substrate. Figures 4(a) and 5(a) are a cross-section along two contacts, and Figs. 4(b) and 5(b) are a cross-section between two contacts. Substrate current distributes in a low-resistivity layer, and there are vertical current flow paths between the substrate surface and low-resistivity layer.



(a) Simulated with doping profile

(b) Simulated with uniform resistivity

Fig. 6. Current density (A/m^2) on substrate surface analyzed with Fig. 2 substrate.



(a) Simulated with doping profile

(b) Simulated with uniform resistivity

Fig. 7. Current density (A/m^2) on substrate surface analyzed with an industrial process.

Figures 6 and 7 show current density at the depth of 1μm from the substrate surface. The current densities simulated with doping profile and uniform resistivity assumption are compared. Figures 6 and 7 indicate that the current distribution spreads smaller range in uniform resistivity assumption. When N-well is placed close to contacts, current distribution is limited. Large contact also restricts the current distribution in comparison with scattered small contacts whose total area is equal to large contact. When two close contacts are placed, the current path on the substrate surface effectively reduces the substrate resistance. Uniform resistivity assumption cannot simulate these limitations or spreading of current distribution, and cause extraction error.

B. Suggestion of substrate resistivity models

It is difficult to extract substrate resistance with doping profile for substrate noise simulation in LSI design. Designers obtain process information from process parameter sheets provided by foundries, which include the interconnect structure, sheet resistance of source/drain area, and so on. However, dop-

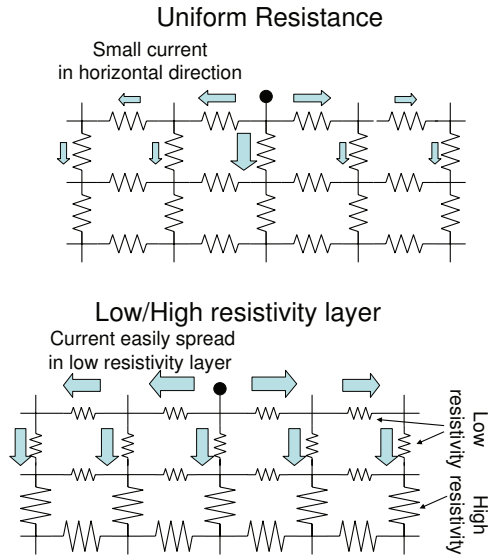


Fig. 8. Current flow in uniform resistivity layer and low/high resistivity layers.

ing profile of substrate is commonly not provided. Fundamental method to acquire the doping profile is process simulation. Measurement of doping profile on silicon is difficult, and simulated doping profile cannot be corrected using measurement results.

We suggest substrate resistivity model which accurately estimates substrate resistance without doping profile. Estimation error of substrate resistance is due to non-uniform resistivity, and one substrate layer can be divided into low-resistivity and high-resistivity layers. Figure 8 depicts that current flows from low-resistivity layer to high-resistivity layer. Current distribution tends to spread in wider range at the low-resistivity layer in comparison with uniform resistivity assumption. Substrate resistivity model needs to include high-resistivity and low-resistivity layers.

We first suggest to approximate doping profile by stepwise resistivity (stepwise model). Stepwise model provides simple approximation of doping profile, but the number of parameters to characterize tends to be large. We also suggest the resistivity model which includes representative resistivity values, the depths of representative resistivity values, and interpolation between representative resistivity values with closed-form expression (interpolation model). The latter model includes smaller number of parameters needed to be characterized than the former model, and characterization of interpolation model is described in Sec. IV..

Table III evaluates the accuracy of the stepwise model and the interpolation model using Tab. II setup. Parameters of models are decided based on doping profile in this evaluation. Stepwise model approximates doping profile with 8 resistivity values, and interpolation model defines resistivity at 3 points. Both stepwise model and interpolation model improve accuracy of substrate resistance extraction in comparison with uniform resistivity assumption in Tab. II. This result indicates that

TABLE III
SIMULATION RESULTS WITH SUBSTRATE RESISTIVITY MODELS. A: EXTRACTED WITH DOPING PROFILE, B: EXTRACTED WITH STEP RESISTIVITY MODEL, C: EXTRACTED WITH RESISTIVITY INTERPOLATION MODEL

No.	Fig. 2 profile			industrial process		
	A	B	C	A	B	C
LAYOUT.1	12771	12830	12768	1242	1239	1354
LAYOUT.2	13163	13332	13284	1313	1322	1425
LAYOUT.3	15822	16402	15115	1380	1369	1472
LAYOUT.4	81433	92937	85985	7042	7837	5998
LAYOUT.5	4027	4312	3774	669	649	715
LAYOUT.6	6049	5328	6868	531	558	578

the models we suggested are effective to estimate substrate resistance accurately.

IV. EVALUATION OF SUGGESTED MODEL

Doping profile of substrate is frequently not provided from foundry, and the substrate resistivity model for substrate resistance extraction is needed to be characterized with measurement results of substrate resistance. Doping profile provided from foundry is a simulated result, and substrate resistivity model is needed to be generated based on simulated doping profile and resistance measurement results. Foundries which cannot provide doping profile also require substrate resistivity model which does not include impurity doping information, and constructed with measured resistance. This section demonstrates the characterization of the substrate resistivity model suggested in Sec. III.B. with substrate resistance.

Here, we demonstrate characterization of the model of p-substrate. The substrate is assumed to be a low-resistivity substrate. The resistivity of surface substrate surface of contact area is acquired from sheet resistance of active area. The parameters of substrate resistivity model is resistivity of surface layer, peak resistivity of epi-layer, resistivity of low-resistivity layer, and the substrate depths where peak resistivity appears and low-resistivity layer starts. Resistivity between surface and peak resistivity depth and between peak resistivity depth and low-resistivity depth are calculated by log-linear interpolation.

We adopted following 11 layout patterns to characterize the model. There are 5 layout types, and each type has 2 or 3 patterns with different dimensions. Layout structures shown in Fig. 3 are applied for following patterns.
- PAT.1.1-1.3: There are sufficiently distant two contacts.
- PAT.2.1,2.2: Two close contacts are placed.
- PAT.3.1,3.2: Two contacts are close to N-well respectively.
- PAT.4.1,4.2: Two contacts are surrounded by N-well respectively.
- PAT.5.1,5.2: Sizes of the two contacts are large.

The goal of characterizing the substrate resistivity model is that substrate resistance values extracted with the fitted model correlate with reference resistance values in these layout patterns. Substrate resistance is extracted by Cadence QRC [14] extractor. Reference resistance values are obtained by extraction with doping profile.

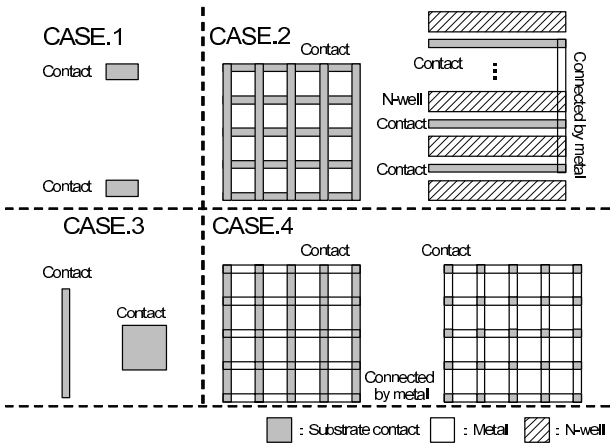


Fig. 9. Layout structures for evaluation.
CASE.1: Two small synchronous contacts.
CASE.2: A contact in a mesh structure and alternatively placed N-wells and contacts.
CASE.3: A long rectangle contact and a large square contact.
CASE.4: Long contacts and scattered small contacts.

Tables IV and V compare reference resistance values, resistance values extracted under conventional uniform resistivity assumption (uniform for each substrate layer), and resistance values extracted with characterized model. Table IV shows results of sample profile in Fig. 2, and results of the industrial process are evaluated in Tab. V. Depth of N-well in Fig. 2 profile is assumed to be 4μm. In addition to patterns for characterization, 4 layout patterns (Fig. 9) which is not used in the characterization were also extracted for evaluation of characterized model. The extraction error is improved in all layout patterns, and average extraction errors of characterized models are 3.5% and 1.4% in Fig. 2 profile and the industrial process respectively. These results indicate that the substrate resistivity model we suggested in this paper can be characterized with substrate resistance, and can be corrected by the resistance measurement results. Substrate resistance can be easily measured with fabricated chips, and the doping profile of fabricated chips is reflected in substrate resistance measured with fabricated chips. The suggested models, which can be characterized with substrate resistance values, can include information of doping profile of fabricated chips.

TABLE IV
EVALUATION FIG.2 DOPING.

Layout pattern	Profile Res.(Ω)	Uniform res. Res.(Ω)	Uniform res. Error (%)	Suggested model Res.(Ω)	Suggested model Error (%)
PAT.1.1	12771	13534	6.0	12666	0.8
PAT.1.2	26137	31990	29.3	29283	12.0
PAT.1.3	13408	14233	11.4	13591	1.4
PAT.2.1	6050	7680	27.0	5848	3.3
PAT.2.2	8811	10612	20.4	8183	7.1
PAT.3.1	15823	13906	12.1	16412	3.7
PAT.3.2	14320	12757	10.9	14861	3.8
PAT.4.1	81433	20024	75.4	76864	5.6
PAT.4.2	28066	12287	56.2	27647	1.5
PAT.5.1	4027	2910	27.7	3775	6.3
PAT.5.2	639	419	34.4	642	0.5
CASE.1	9737	9728	0.1	9533	2.1
CASE.2	177	96.7	45.2	173	2.2
CASE.3	4900	4456	9.1	4892	0.1
CASE.4	578	480	17.0	588	1.6

TABLE V
EVALUATION WITH AN INDUSTRIAL PROCESS.

Layout pattern	Profile Res.(Ω)	Uniform res. Res.(Ω)	Uniform res. Error (%)	Suggested model Res.(Ω)	Suggested model Error (%)
PAT.1.1	1406	1513	7.6	1397	0.7
PAT.1.2	2703	4301	59.1	2651	1.9
PAT.1.3	1541	1598	3.7	1524	1.1
PAT.2.1	570.5	1019	78.6	557	2.4
PAT.2.2	874.9	1309	49.6	864	1.3
PAT.3.1	1850	1489	19.5	1838	0.6
PAT.3.2	1645	1377	16.3	1639	0.4
PAT.4.1	9320	1690	81.9	8726	6.4
PAT.4.2	3034	1247	58.9	3029	0.2
PAT.5.1	451.7	216	52.1	455	0.6
PAT.5.2	73.96	22.6	69.4	75.4	2.0
CASE.1	1074	1045	2.7	1070	0.4
CASE.2	20.27	7.34	63.8	20.50	1.1
CASE.3	555.9	434	21.9	556	0.0
CASE.4	63.29	39.0	38.4	64.8	2.3

V. CONCLUSION

This paper presented that the general assumption where resistivity of each substrate layer is regarded to be uniform causes extraction error of substrate resistance. The extraction errors were observed in layout patterns of large contacts, close contacts, and contacts close to N-well.

We suggested the stepwise resistivity model and the interpolation model. These models include non-uniformity of substrate resistivity and provide fine approximation of doping profile. The extraction results of substrate resistance with these models show fine correlation with extraction results with doping profile.

Characterization of suggested model was also demonstrated. The suggested interpolation model was characterized with reference substrate resistances which can be easily obtained with measurement on the fabricated chips. The resistance extraction results with characterized model accurately estimated substrate resistance of layout patterns where estimation with uniform resistivity model causes extraction errors. The suggested model can be characterized with measured substrate resistance values without doping profile.

REFERENCES

[1] M. D. Wilde, W. Meeus, P. Rombouts, and J. V. Campenhout, "A Simple On-Chip Repetitive Sampling Setup for the Quantification of Substrate Noise," *IEEE JSSC*, vol. 41, no. 5, pp. 1062–1072, May 2006.

[2] M. V. Heijningen, J. Compiet, P. Wambacq, S. Donnay, M. G. E. Engels, and I. Bolsens, "Analysis and Experimental Verification of Digital Substrate Noise Generation

for Epi-Type Substrates," *IEEE JSSC*, vol. 35, no. 7, pp. 1002–1008, July 2000.

[3] D. Kosaka, M. Nagata, Y. Murasaka, and A. Iwata, "Chip-Level Substrate Coupling Analysis with Reference Structures for Verification," *IEEE Trans. on Fundamentals*, vol. E90-A, no. 12, pp. 2651–2660, Dec. 2007.

[4] M. Nagata, J. Nagai, T. Morie, and A. Iwata "Measurements and Analyses of Substrate Noise Waveform in Mixed-Signal IC Environment," *IEEE TCAD*, vol. 19, no. 6, pp. 671–678, June 2000.

[5] S. Kristiansson, F. Ingvarson, S. P. Kagganti, N. Simic, M. Zgrda, and K. O. Jeppson, "A Surface Potential Model for Predicting Substrate Noise Coupling in Integrated Circuits," *IEEE JSSC*, vol. 40, no. 9, pp. 1797–1803, May 2005.

[6] X. Wang, W. Yu, and Z. Wang, "Efficient Direct Boundary Element Method for Resistance Extraction of Substrate With Arbitrary Doping Profile," *IEEE TCAD*, vol. 25, no. 12, pp. 3035–3042, Dec. 2006.

[7] C. Xu, R. Gharpurey, T. S. Fiez, and K. Mayaram "Extraction of Parasitics in Inhomogeneous Substrates With a New Green Function-Based Method," *IEEE TCAD*, vol. 27, no. 9, pp. 1595–1606, Sep. 2008.

[8] A. Samavedam, A. Sadate, K. Mayaram, and T. S. Fiez, "A Scalable Substrate Noise Coupling Model for Design of Mixed-Signal IC's," *IEEE JSSC*, vol. 35, no. 6, pp. 895–904, June 2000.

[9] O. Valorge, C. Andrei, F. Calmon, J. Verdier, C. Gontrand, and P. Dautriche, "A Simple Way for Substrate Noise Modeling in Mixed-Signal ICs," *TCAS-I*, vol. 53, no. 10, pp. 2167–2177, Oct. 2006.

[10] W. K. Chu, N. Verghese, H.-J. Chol, K. Shimazaki, H. Tsujikawa, S. Hirano, S. Doushoh, M. Nagata, A. Iwata, and T. Ohmoto, "A Substrate Noise Analysis Methodology for Large-scale Mixed-Signal ICs," in *Proc. IEEE CICC*, pp. 369–372, 2003.

[11] H. Li, C. E. Zemke, G. Manetas, V. I. Okhmatovski, E. Rosenbaum, and A. C. Cangellaris, "An Automated and Efficient Substrate Noise Analysis Tool," *IEEE TCAD*, vol. 25, no. 3, pp. 454–468, Mar. 2006.

[12] R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE JSSC*, pp. 344-353, vol. 31, no. 3, Mar. 1996.

[13] S. M. Sze, "Chapter 13 Impurity Doping," in *Semiconductor Devices: Physics and Technology*, 2nd ed., Wiley, 2001.

[14] Cadence Design Systems Inc., "QRC Extraction Users Manual, Product Version 10.1.3 HF1," Oct. 2011

[15] Synopsys Corp., "Raphael Interconnect Analysis Program Reference Manual, Version D-2010.03," Mar. 2010