A Third Order Delta-Sigma Modulator with Shared Opamp Technique for Wireless Applications

Ghazal Fahmy¹, Daisuke Kanemoto¹, Haruichi Kanaya¹, Ramesh Pokharel² and Keiji Yoshida¹
¹ Graduate School of Information Science and Electrical Engineering, ² EJUST Center,
¹,² Kyushu University, 744, Motooka, Fukuoka, 819-0395, JAPAN
E-mail: ghazal@yossvr3.ed.kyushu-u.ac.jp

Abstract — this paper described the design of a third order delta-sigma modulator (DSM) exploited shared opamp technique in order to reduce number of opamp required, consequently the total power consumption for the modulator decreased as well as required area decreased too. The architecture relaxed comparator speed which appropriate for wireless applications. First and second stages are sharing one opamp in integration and sampling phase. The proposed circuit has been designed on TSMC 0.18μm CMOS technology. 2MHz Bandwidth, 50dB Peak Signal-to-Quantization-Noise Ratio (SQNR), which is suitable for WCDMA, have been achieved. It consumes 2.4mW with power supply 1.2V and area is 0.3mm².

I. INTRODUCTION

High order loop filter is one of conventional approach to attain high resolution delta-sigma modulator (DSM) which required an opamp for each integrator. The conventional third order 1-bit DSM required three amplifiers. However, amplifier is only used in one phase of clock period for signal integration. In order to use two phases of clock period for signal integration without increasing in the supply current of amplifier, there are two approaches: one is “double sampling switch capacitor (SC) integrator which increase over sampling ratio(OSR) and other is time sharing technique which increase DSM order. The advantages of time sharing technique are decreasing number of opamp required for the same order, low power consumption, no mismatching in sampling capacitor like double sampling technique [1] and low area. Time sharing amplifier technique has been previously published in SC filters, DSM for audio applications [2]. A DSM for audio applications has been employed a third order DSM using one opamp [3], it requires a very high speed quantizer which is very difficult to implement in wireless applications. In order to relax the quantizer speed, one more opamp has been adding for third integrator. Moreover, feed-forward technique has been applied to relax the performance of analog component [4].

This design targets to WCDMA applications that required the highest bandwidth 1.92MHz and over 50dB SQNR. In this paper a proposed third order, feed-forward, and 1-bit quantizer DSM with two opamp is presented. Shared-amplifier technique for first and second integrator has been provided. The proposed circuit has been simulated using TSMC 0.18μm process.

II. PROPOSED CIRCUIT AND DESIGN SIMULATION

Fig. 1 illustrates fully-differential circuit schematic of the proposed DSM. The circuit is composed of two opamps, an analog adder and 1-bit quantizer. The first opamp is used to realize first and second integrator. It is required T/2 to perform integration for each stage. Cs1 and Cs2 are a sampling capacitor for the first and second integrator respectively, in addition, Ci1 and Ci2 are integration capacitor for third and second integrator correspondingly.

The second opamp realized third integrator using Cs3 and Cs3 for sampling and integration phase respectively which required half cycle for each phase, therefore the comparator has adequate time to make decision. Ca1, Ca2, Ca3 and Ca4 have been used to implement a passive analog adder for 1-bit quantizer. Q1 and Q2 are non-overlapped clock, Q1d and Q2d are delayed clock for Q1 and Q2 respectively. Fig. 2 show the timing diagram for each stage of the proposed circuit. When Q2 is high, the input signal is sampled by Cs1, during the sampling phase for the first stage, the first opamp is busy in integration for the second stage. The capacitor charge of Cs2 transferred to Ci3 then sampled by Cs3. When Q1 is high, the capacitor charge of the Cs1 transferred to Ci1 then sampled by Cs2. The passive adder summed the charges when Q1 is high except the charges come from second stage that inverted and transferred to Cs3 when Q2 is high. The output of the passive adder was quantized by the comparator when Q1 is high.

The proposed DSM circuit is designed on TSMC 0.18μm technology with 1.2V supply. The circuit has been design in fully differential. Sampling clock (Fs = 80MHz) has been used to generate non-overlapped clock (Q1, Q2). Bandwidth and DC gain for the opamp were designed to be 250MHz and 45dB respectively and power consumption is 1.1mW that meet the requirements of WCDMA specifications. The output spectrum of circuit simulation with -6dBFS sine-wave with 500KHz input frequency has been illustrated in Fig.3. Table 1 shows the result summary of proposed circuit compared to other result using [5]. Where P is power consumption, N is the effective number of bits Fb is the signal bandwidth The Figure of Merit (FoM) of the modulator was written as following:

\[ FoM = \frac{P}{2^N \cdot 2 \cdot F_B} \] (1)
Fig. 1 proposed circuits for 3rd order DSM Modulator.

Table I Performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[5] 2009 (ISSCC)</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>1.2v</td>
<td>1.2v</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18μm</td>
<td>0.18μm</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>80MHz</td>
<td>80MHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>2MHz</td>
<td>2MHz</td>
</tr>
<tr>
<td>SQNR</td>
<td>58dB</td>
<td>50dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>6.43mW</td>
<td>2.4mW</td>
</tr>
<tr>
<td>FoM (P/\text{fs}[\text{pJ}])</td>
<td>2.47</td>
<td>2.32</td>
</tr>
</tbody>
</table>

Table 1. Shows the design parameter and result of the proposed design that attains a FoM of 2.32\text{pJ}/\text{Conv. Step} which is lesser than [5] the modulator achieves a lower figure of merit. Fig.4 shows the circuit’s simulation power spectrum density. Fig.5 shows layout of the proposed circuit and clock generator which is 0.3mm2.

Fig.3 Output spectrum of spectre circuit simulation.

III. CONCLUSION

Shared amplifier technique has been applied in a third order DSM to decrease number of amplifiers required. Moreover, decrease the power consumption. The proposed DSM has been designed and simulated employing OSR=20. The proposed DSM has achieved SQNR 50dB for -6 dBFS, 2.4mW power dissipation, and 2MHz bandwidth.

ACKNOWLEDGMENT

This work was partly supported by a Grant-in-Aid for Scientific Research from JSPS (KAKENHI), a researcher grant from the Mazda Foundation, and Fukuoka project in the Cooperative Link of Unique Science and Technology for Economy Revitalization (CLUSTER) from Ministry of Education, Culture, Sports, Science and Technology (MEXT). This work was also partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent.

REFERENCES