Power optimization of a micro-controller with Silicon On Thin Buried Oxide

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Abstract— From battery supplied mobile devices to supercomputers, reducing the power consumption has become a serious design issue. Although using low power supply is the most efficient way to reduce the power, it also increases the leakage power and delay variance. Low-power Electronics Association & Project(LEAP) developed Silicon On Thin Buried Oxide(SOTB) technology to solve those problems. In order to verify the SOTB technology, a microcontroller V850E-Star is implemented. In this paper, we investigate the operational speed and leak power with 40 kinds of reverse bias and forward bias voltages for each purpose: standby, energy maximum and performance maximum. In the standby mode, leak power of the energy maximum mode is reduced by 92%, while it works with 33MHz frequency clock in the energy maximum mode.

I. Introduction

Nowadays, from battery supplied mobile devices to supercomputers, reducing the power consumption has become a serious design issue. Also it becomes impossible to disregard the problem of leakage power as device scaling progresses, and it has become a stage irreducible without the sacrifice of performance. Furthermore, low V_{th} has reached the limit by the increase in variation of the threshold voltage V_{th}. The main reasons of the variation in V_{th} are not only the thinness of layer or lithography variation but also line edge roughness (LER) and random dopant fluction (RDF) are concerned greatly. Especially the variation in V_{th} by RDF is becoming a problem with advancing of the process technology. Although using low power supply is the most efficient way to reduce the power, it also increases the leakage power and delay variance.

In order to solve this problem, Low-power Electronics Association & Project (LEAP) developed Silicon On Thin Buried Oxide (SOTB) technology. Moreover, in transistors using the SOTB, the control range of back gate is wide. It is possible to optimize the performance and power consumption after the fabrication, and it works with low power supply voltage: V_{dd}.

A single chip microcontroller Renesas's V850E-Star is widely utilized for embedded systems including car electronics, one of the most attractive target fields of low leak process. In this paper, we implemented V850E-Star with SOTB technology, and show the reduction of power consumption with low V_{dd}. In addition, we control the speed and leak of microcontroller by controlling back-gate bias, and show how bias voltage should be set up. Here, we considered the following three modes according to a use.

- Standby mode - reduce the leak as possible.
- High speed mode - high performance computation.
- Balance mode - optimize the energy consumption.

II. SOTB

In this section, the technology of Silicon on thin Buried OXide (BOX) is introduced. This technology[1][2] has been developed by Low-power Electronics Association & Project(LEAP)[3].

A. SOTB CMOSFET

Design of the threshold voltage must be determined to balance between performance and leakage power considering the use of LSI. By using conventional bulk CMOS, it is difficult to find the acceptable value in the limitation. The Silicon on Insulator (SOI CMOS) technology has attracted attention from the viewpoint of balancing the performance and leakage power with the low voltage supply. Unlike traditional bulk CMOS shown in Figure 1, in SOI, transistors are formed on top of the insulator(typically SiO_2)in SOI CMOS (Figure 2. By making the transistor in a way that is surrounded by insulating material, the electrical interference is not needed to consider, and the electric characteristics become sharp.[1] There are two types of SOI: FD(Fully Depleted)-SOI and PD(Partially Depleted)-SOI. Although the process of FD-SOI is relatively difficult, the benefits of SOI can be fully available. The SOTB (Silicon on thin BOX) utilized here is classified into FD-SOI.

Figure3 shows the cross-sectional diagram of SOTB/bulk hybrid design[4][5].

By using an ultra-thin FD-SOI layer and the BOX layer, short channel effect (SCE) is suppressed in the SOTB. Since the impurity doping (halo implant) to channel is not necessary, the variation of threshold voltage by the RDF can be reduced. Multi-threshold voltage design is easily available by doping an impurity into the substrate directly under the thin BOX layer. Thus, it can

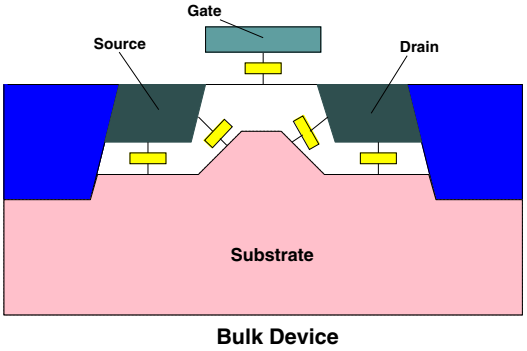

Fig. 1. Cross-sectional view of Bulk Device

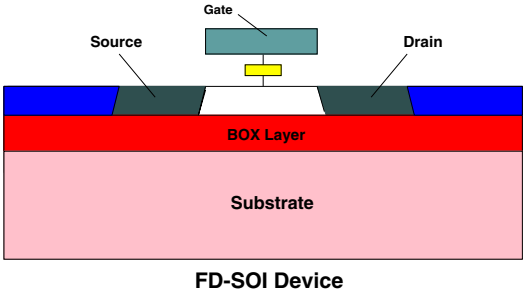

Fig. 2. Cross-sectional view of the FD-SOI Device

widely control the range of back-gate bias and can realize optimization of performance and power consumption after fabrication.

One of the drawbacks of FD-SOI structure is that the electrostatic discharge sensitivity is poor resulting the small breakdown voltage. This can be solved easily by using bulk technology into the same wafer as shown in Figure 3. The manufacturing process can easily incorporate bulk CMOSFET by removing the thin SOI layer and the BOX layer. Also the transistor and the independence of the back-gate are guaranteed by the shallow-trench-isolation (STI). Although STI is almost similar to those used in the bulk device, the three layers of SOI, BOX and the substrate are etched by STI. The well area under the BOX layer behaves as a ground plane and back-gate with a contact. In order to avoid the leakage when applying a back-gate bias, the triple-well structure is introduced.

B. *Characteristics of SOTB*

The SOTB has the following characteristics. First, junction capacitance of the SOI is about 1/10 of that of bulk, and so high-speed operation is possible. Capacitance of the circuit will become large as junction capacitance increases, and the operation speed becomes slow. The benefits of SOI will grow significant for the low voltage operation. Second, one of the main problem of CMOS device, latch-up which has a risk to destroy the device does not occur. Latch-up is caused by a parastic thyristor formed by adjacent transistors in bulk CMOS but they are not formed in SOI. Third anti-radiation tolerance is

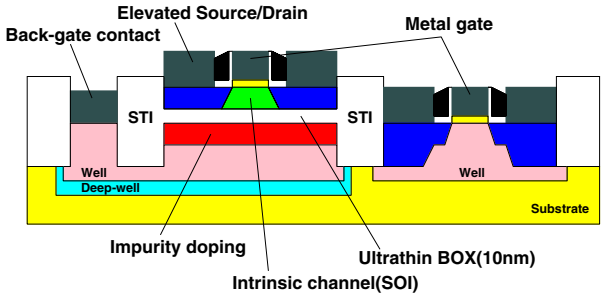

Fig. 3. Cross-sectional view of the SOTB

high. Charge-generating substrate part by the incident radiation is blocked by the insulation layer, and does not affect the operation of the circuit. Fourth, noise propagation (cross-talk) is small because of the insulation. Last, since thermal conductivity of insulation substrate is small, heat dissipation is not so good.

The last item is not so important problem when the chip is used for low power processing.

III. V850E-Star

A. *Specification of mounted V850E-Star*

V850E-Star[6] is a 32-bit microcontroller which is developed by Renesas. It is a RISC processor with a simple 5-stage in-order pipeline suitable for a real time processing. Instructions are extended for application of digital-servo control, such as multiply instruction, saturate calculation, bit manipulation command, and etc. by providing a hardware multiplier.

Since it was a prototype for SOTB implementation, common structures such as instruction/data cache, interrupt mechanism, and a DMA control unit were omitted. Instead, it has instruction memory (VFB_RAM) and data memory (VDB_RAM) which is 128Kbyte each as an on-chip local memory. It provides CSI as an external interface which can be used to load of the test program to CPU macro and read-out of results of the tests. Moreover, an external bus to connect with FPGA placed outside the chip is also provided.

B. *CPU Structure*

Figure 4 shows the block diagram of the implemented chip.

It is consisting of the following modules. With a CPU core, almost all instruction processing, such as address computation, an arithmetic logical operation, and data transfer, is performed by a 1-clock throughput by five-step pipeline control. In Bus Control Unit, a required bus cycle is started based on the physical address obtained by CPU. In Bus Bridge, conversion of the signal for system buses and the signal for peripheral equipment is performed. In V850E-Star Internal Peripherals, it is a register for built-in resources, such as a bus size setup and a wait setup. In Debug Control Unit, communication by

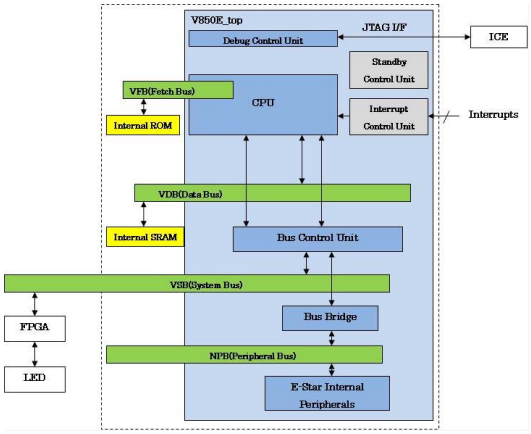

Fig. 4. CPU block configuration

JTAG I/F and execution of debugging processing on an on-board are controlled.

C. Memory configuration

Next, the memory configuration of this chip is introduced.

The right to access of each domain is shown below.

- VFB_RAM for instructions.
  - Only Read is possible from CPU, and
  - read and Write are possible from CSI.
- VDB_RAM for data.
  - Read and Write are possible from CPU and CSI.
- External FPGA memory.
  - Read and Write are possible from CPU and CPI.
- Circumference registers.
  - Read and Write are possible from CPU.
- CSI register.
  - Read and Write are possible from CSI
- Reserved.
  - Access denied

VFB_RAM, VDB_RAM, and external FPGA domain can be accessed exclusively only by the master set up the right to access by the CSI register setup. Moreover, about Reserved, the operation at the time of accessing is not guaranteed.

D. Chip implementation

Implementation of the chip evaluated in this paper carried out by the tools shown in Table I

The layout of V850E-Star is shown in Figure 5. The chip evaluated in this paper is using the transistor of the

TABLE I
DESIGN ENVIRONMENT

Library	LEAP65nm/LPT-3
Logic Synthesis	Design Compiler
Routing of Layout	IC Compiler
Simulation	Mentor ModelSim | Synopsys HSIM
Verification	Mentor Calibre
Package	208PIN QFP
Voltage	0.4V - 1.2V

bulk system corresponding to the right portion of Figure 3, and it is not SOTB itself. One of the advantages of SOTB is that the mixture with a bulk system is possible, and design rules are the same. Even if it is a cell of a bulk system, of course, the control by back-bias is possible. The structure of V850 E-Star is the same as the full-scale SOTB version now under evaluating.

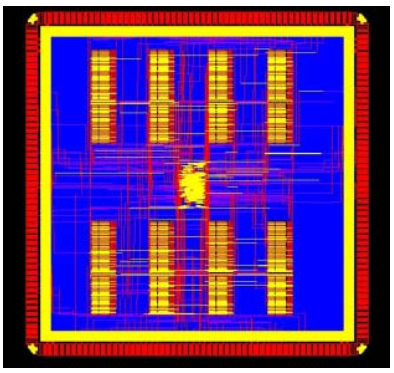

Fig. 5. Layout of V850E-Star

The CPU main part occupies the small domain in the central part, eight surrounding rectangles are memories which are 32Kbytes each and four are used as VDB_RAM and another are used as VFB_RAM, and they constitute 32-bit width.

IV. EVALUATION

The purposes of this research are to evaluate the electric power and clock frequency of V850Estar at the time of hanging substrate bias, and to find for the bias voltage according to a use, and to clarify the clock frequency and electric power at that time. For this goal, two, simulation evaluation and real chip evaluation, were performed. Note that simulation results are based on SOTB transistors, while the real chip evaluation uses bulk transistors.

A. Evaluation by a simulation

LEAP65nm was characterized with zero bias, and analyzed by PrimeTime or Design Compiler of Synopsys as a common LSI design flow. The post layout simulation can be done with the above environment. However, the method cannot be used to estimate the delay and leakage current when back-bias is changed. By using high speed

circuit simulators, both can be evaluated if the target circuit is small. However, V850E-Star is a 32-bit processor which requires too much time to simulate with various bias voltage and clock frequency.

Thus, we evaluated them by the following methods.

- Using PrimeTime of Synopsys, the critical path of the microcomputer was extracted and the cell on the path was analyzed. Result shows that it contains six cells (clockbuffer, D-type flip-flop, inverter, NAND, NOR, and repeater). About these six cells, the delay time with each bias voltage was measured by circuit simulator HSIM, and maximum operating frequency was calculated from this.

- Since only DC analysis was enough to evaluate the leakage power, where bias is applied to the whole chip, it measured by performing a circuit simulation.

Here, 40 kinds of forward bias and reverse bias were used in this evaluation.[7] The back-bias (substrate voltage) VBP is given to pMOS transistor, and the back-bias VBN is given to nMOS transistor. The substrate (well) is p type and source is n type in nMOS. Since it takes electric potential of 0V, it becomes forward bias when the voltage is higher than 0 is given and becomes reverse bias when the voltage which is lower than 0 is given (vice versa for pMOS). Then, when power supply voltage is set to 0.4V this time, VBP=0.4V and VBN=0V are a zero bias state. In the direction of reverse bias, VBP is raised to 0.01 units, VBN is lowered, and a total of 40 kinds of bias until it is finally set to VBP=0.8V and VBN=-0.4V. In the direction of forward bias, VBP is similarly lowered to 0.01 unit voltage, VBN is raised, and the bias of 40 kinds of totals until it is set to VBP=0V and VBN=0.4V. When power supply voltage was 0.8V, bias was changed with the 0.02V unit voltage.

B. *Measurement result of delay and leak*

Figure 6 shows the relation of bias-delay of six cells (clockbuffer, D-type flip-flop, inverter, NAND, NOR, and repeater) with the power supply voltage 0.4V, and Figure 7 shows leakage current of the CPU core.

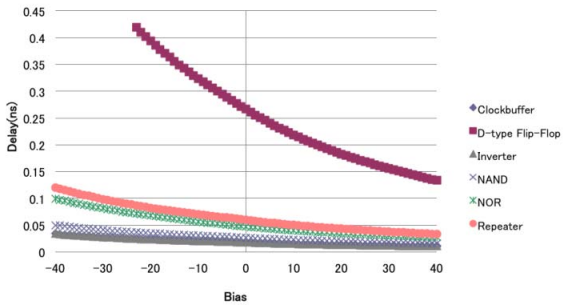

Fig. 6. The relationship between bias and delay with $V_{dd} = 0.4V$

A measurement result shows that delay and leakage current are well controllable by substrate bias. In order for

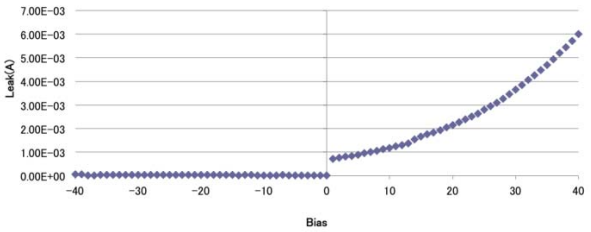

Fig. 7. The leakage current with $V_{dd} = 0.4V$

power supply voltage to reduce leak most in 0.4V, it turns out that what is necessary is just to use VBN=-0.24V. When reverse bias was applied rather than VBN=-0.24V in D type flip-flop, it did not operate normally. Therefore, this voltage should be used in the Standby mode. On the other hand, the forward bias for being delayed short is a limit about VBN=0.4V, and made this voltage the fast mode.

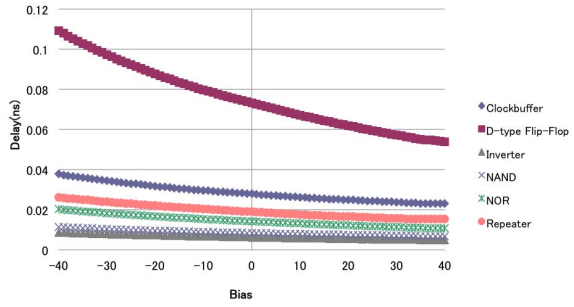

Fig. 8. The relationship between bias and delay with $V_{dd} = 0.8V$

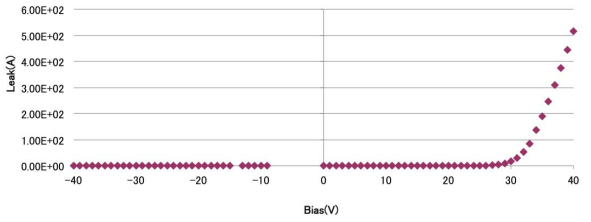

Fig. 9. The leakage current with $V_{dd} = 0.8V$

On the other hand, Figure 8 shows the relation of bias-delay of six cells (clockbuffer, D-type flip-flop, inverter, NAND, NOR, and repeater) in the supply voltage 0.8V, and Figure 9 shows leak of the chip. Similarly, power supply voltage made bias of Standby mode VBN=0.8V, and fast mode for the bias of VBN=-0.8V in 0.8V.

C. Consumption energy minimization

There are many ways to optimize the power consumption. Here, the Balance mode which minimizes the energy consumption during the operation is investigated from the evaluation results. Dynamic electric power is obtained from the usual after-layout real delay simulation, and this electric power is hardly affected by the back-bias. The leakage current of a measurement result is added to this, the whole electric power is found, and delay is applied to it. Energy is computed and let the lowest bias of energy be Balance mode. As a result, in $V_{dd} = 0.4V$, the bias of VBN=-0.42V turned into bias of VBN=-0.14V, and became Balance mode by $V_{dd} = 0.8V$. The formula of energy calculation is shown below.

$$E = (P_{leak} + P_{dynamic}) \times T_{delay} \quad (1)$$

D. Frequency evaluation

Figure 10 shows the frequency of Balance mode and fast mode.

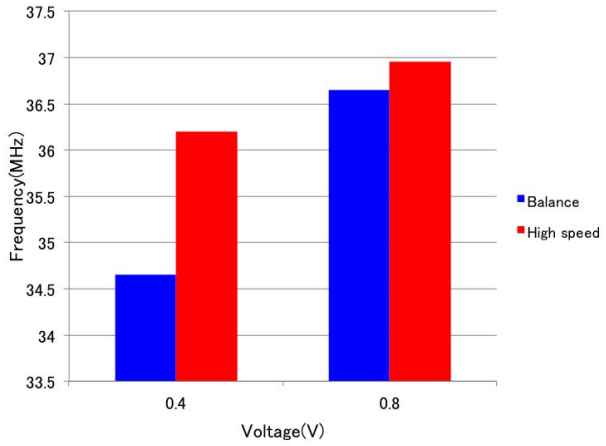

Fig. 10. The frequency of Balance mode and High speed mode in each voltage

In the voltage 0.4V, 34.65MHz was measured in Balance mode, and 36.20MHz was measured in the fast mode. In the voltage 0.8V, 36.65MHz was measured in Balance mode, and 36.95MHz was measured in the fast mode. At 0.8V, the increase in the frequency was not able to be expected by the high forward bias voltage.

E. Leak evaluation

Figure 11 shows the leak of Balance mode and the Standby mode.

In the voltage 0.4V, it measured 37.9μA was measured in Balance mode, and 15.8μA in the Standby mode. In the voltage 0.8V, it measured 39.5μA in Balance mode, and 0.334μA in the Standby mode. It is because Balance mode is in a reverse bias direction rather than when the voltage 0.4V as a factor with less power supply voltage 0.8V to leak.

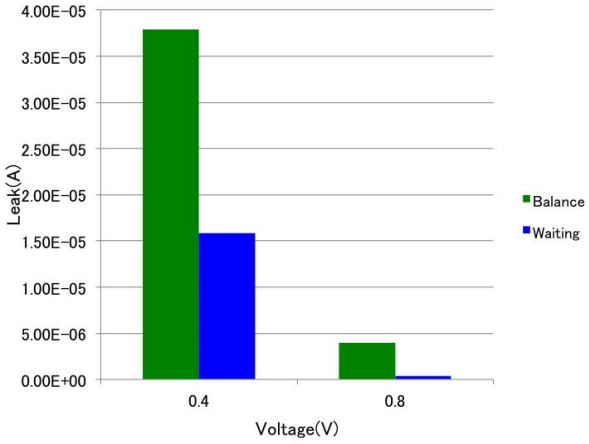

Fig. 11. The leak of Balance mode and Standby mode in each voltage

V. Real chip evaluation

We evaluated the operational frequency and the leakage current with a real chip. Note that the real chip uses bulk-transistor instead of the SOTB, and so it does not work with 0.4V supply voltage. All evaluation is done with a supply voltage is 0.8V. Figure 12 shows the real chip which we used at evaluation. A simple program just to check the CPU operation is used. Figure 13 shows the relation between bias and leak, Figure 14 shows the relation between bias and frequency, and Figure 15 shows the power optimization at real chip in 0.8V.

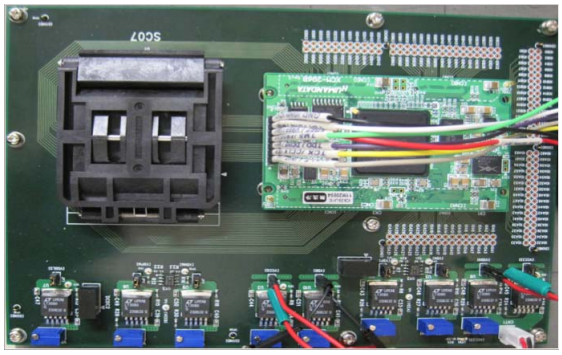

Fig. 12. Test board for the real chip

From these results, it appears that the leakage can be controlled by substrate bias, like a simulation results. However, in Figure 14, the evaluation more than 0.18V was impossible because of a rapidly increasing leak.

Here, Standby mode is using VBN=-0.16V, and High speed mode is with VBN=0.16V.

Furthermore, we tried to find Balance mode by the same way as a simulation. As a result, Balance mode becomes when VBN=0.12V as you can see in Figure 15.

In frequency evaluation, it was measured 25MHz in Standby mode, 53MHz in Balance mode, and 53MHz in High speed mode. In leak evaluation, it was measured

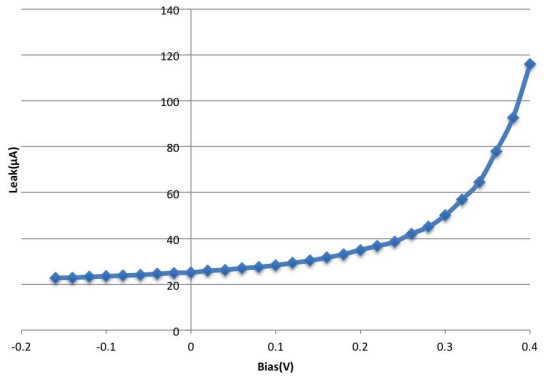

Fig. 13. The relationship between bias and leak at real chip

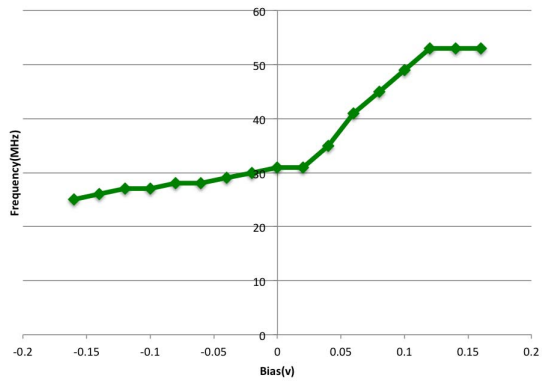

Fig. 14. The relationship between bias and frequency at real chip

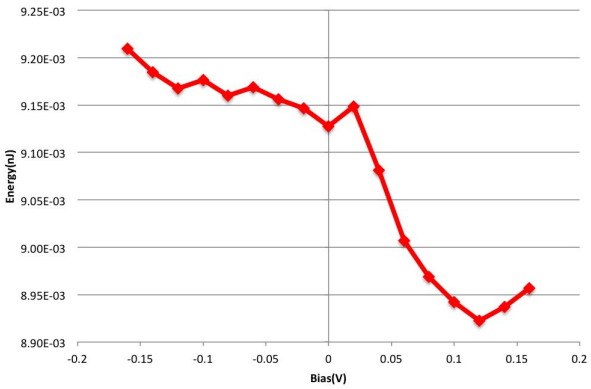

Fig. 15. Power optimization at real chip

$22.8\mu A$ in Standby mode, $29.3\mu A$ in Balance mode, and $31.6\mu A$ in High speed mode.

VI. Conclusion

In this paper, we implemented V850E-Star microcontroller for embedded systems using the prototype bulk transistor of the SOTB process by FD-SOI technology, and evaluated the influence of delay and leak by substrate bias. As a result, in High speed mode, 4% of increase in speed was achieved compared to Balance mode at maximum, and 92% reduction of leak was achieved to Balance mode in Standby mode.

Here, a chip using bulk transistors is evaluated with high (0.8V) supply voltage, while simulation results are based on SOTB transistors with low (0.4V) supply voltage. In both cases we found the back-gate bias voltages for Standby, Balance and High speed mode. By using such bias voltage values, various trade-off between operational speed and leakage current can be realized.

Now, a new chip with fully SOTB transistors is under evaluating. We will report about the difference of real chip evaluation results between SOTB and bulk transistors.

Acknowledgment

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