Hardware Acceleration Technique for Radio-resource Scheduler in Ultra-high-density Distributed Antenna Systems

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Abstract - This paper presents a hardware acceleration technique for the scheduling process in ultra-high-density distributed antenna systems for 5G mobile communications systems. In 5G systems, the overall system throughputs for a huge number of combinations of antennas and user equipment for communications have to be calculated in the scheduling process. In order to accelerate the calculation, the proposed technique calculates the throughputs of each UE simultaneously. Moreover, it obtains the system throughput for combinations at every clock cycle in the pipeline. Experimental results show that the proposed technique performs the calculation of system throughput 60 times faster than without the acceleration. The proposed technique enables a future practical 5G system.

I. Introduction

In mobile communications systems, the resource scheduling process controls radio transmission for all antennas. In the process for downlink transmission, user equipment (UE) is assigned to each antenna [1]. Before the fifth generation of mobile communications systems (5G), this assignment will have been executed by software-based processing because of a small number of antennas, as shown in Fig. 1(a), and a small number of possible combinations of antennas and UEs.

In 5G system, in order to increase the overall system throughput, a huge number of antennas will be deployed in ultra-high density [Fig. 1(b)], [2]. The number of possible combinations reaches approximately 10^{76} when the numbers of antennas and UEs are 32 and 256, respectively, which is based on a 5G-system model in mobile and wireless communications enablers for the twenty-twenty information society (METIS) [3].

In order to obtain the suitable combination from this explosive increase of possible combinations, an approximate search has been reported [4]. In general, an approximate search can approach the suitable combination as the number of searched combinations increases. However, it will be difficult to increase the number of searched combinations by software-based processing within the limited scheduling period of 1 ms [5] because of the limitation of the number of CPU cores.

To overcome this issue, we propose a hardware acceleration technique that enables the scheduler to accelerate the scheduling process in ultra-high-density distributed antenna systems.

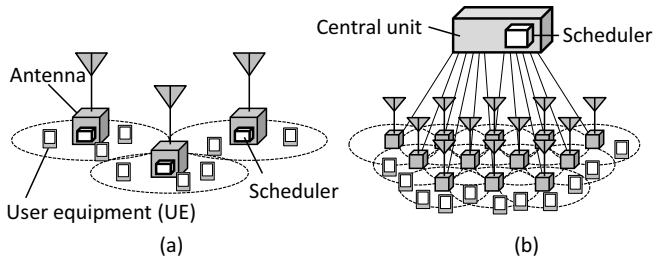

Fig. 1. Illustrations of antenna deployment (a) before the 5G system and (b) in the 5G system (ultra-high-density distributed antenna systems).

II. Proposed Technique

Figure 2 shows our proposed acceleration technique for the scheduling process. In this technique, the search process is executed by a dedicated circuit in order to increases the number of searched combinations, which improves the scheduling performance. The software sets possible UEs for each antenna to the hardware accelerator before starting the search process. The details of the hardware acceleration technique are described below.

A. Hardware Accelerator

1) Approach

Figure 3 shows the flow of the search process performed by the hardware accelerator. First, the combination of antennas and UEs is generated. Next, the system throughput is calculated by summing the throughputs of all of the UEs in the generated combination. Then, the combination for which the scheduling achieves higher system throughput is decided by comparing the system throughput for each combination. These three steps are iterated until the scheduling period expires so that the suitable combination can be obtained.

To clarify the steps that should be accelerated in the above search process, we investigated the processing time for each step. According to the investigation by software-based processing, the system-throughput calculation accounts for more than 90 % of the processing time to execute the search process. On the basis of the results, we devised a parallel and pipeline processings for accelerating the system-throughput calculation.

2) Detail of hardware accelerator

Figure 4 shows a block diagram of the circuit. The circuit comprises three parts: a combination-generation part that outputs the combination of antennas and UEs, a system-throughput-calculation

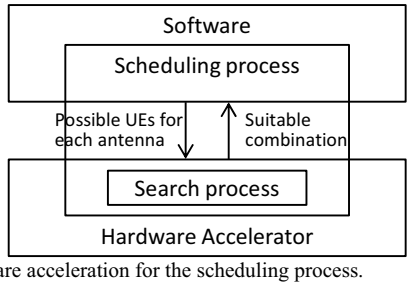

Fig. 2. Hardware acceleration for the scheduling process.

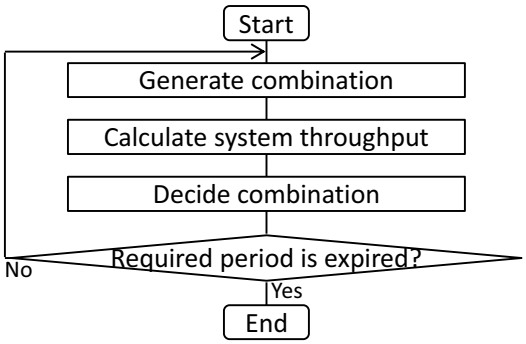

Fig. 3. Flow chart of the search process.

part, and a combination-decision part that decides the combination by comparing the system throughput for each combination. Our proposal consists of two kinds of processing: parallel processing for calculating the throughput for all UEs simultaneously and pipeline processing for obtaining the system throughput for generated combinations at every clock cycle.

The system-throughput-calculation part consists of plural throughput-calculation blocks that output the throughputs of the UEs in parallel. The throughput-calculation blocks are provided with the same number of antennas. The throughput-summation block outputs the system throughput by summing the throughputs of the UEs. The throughputs of the UEs are simultaneously calculated at the throughput-calculation blocks. Hence, the circuit executes the search process at high speed. Furthermore, the circuit scale can be minimized by optimizing a parallel number for the same number of antennas.

Figure 5 shows the timing chart of the system-throughput-calculation block. In this block, the received signal power to interference power and noise ratio (SINR) is calculated. Next, the calculated SINR is converted to the throughput. Then, the throughputs of the UEs are summed. These steps are independent of the previous and next combinations. Therefore, these steps are executed in the pipeline. This enables the scheduler to obtain the system throughput for generated combinations at every clock cycle.

III. Performance Evaluation

In order to evaluate the performance of the proposed technique, we carried out experimental measurements. To verify the number of searched combinations within the scheduling period of 1 ms, we measured the processing time spent for the search process.

The proposed technique was implemented on a field-programmable gate array (FPGA) (Xilinx Zynq-7045) at the clock frequency of 100 MHz. The processing time was measured with the FPGA. The processing time without acceleration was measured with a general purpose processor (Intel Core i5) at the clock frequency of 2.67 GHz.

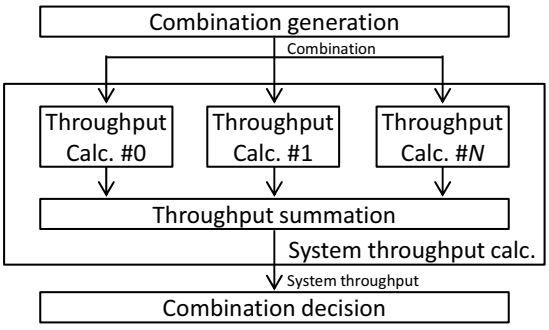

Fig. 4. Circuit block diagram.

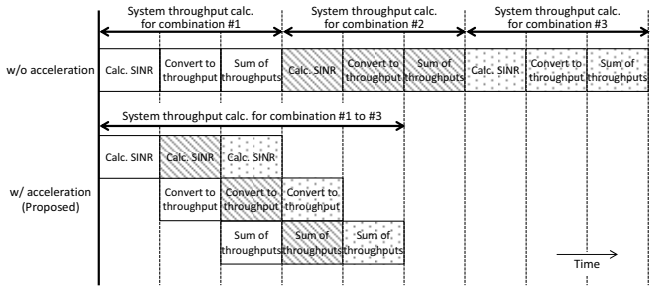

Fig. 5. Timing chart.

Table I shows the results of the performance evaluation. The processing time per searched combination measured with acceleration is 10 ns. The processing time without acceleration is 596 ns. The circuit executes the search process about 60 times faster than without acceleration. From these results, the number of searched combinations within the scheduling period of 1 ms in the proposed technique is 10^5 and that in the processing without acceleration is 1679. These results show that the number of searched combinations in the proposed technique is about 60 times larger than without the acceleration.

Furthermore, we carried out system-level simulations for the evaluation of the system throughput. The proposed technique achieves about 73 % improvement of the system throughput when the number of antennas and UEs are 32 and 256, respectively. Consequently, the proposed technique enables the scheduler to obtain the suitable combination in ultra-high-density distributed antenna systems.

TABLE I. Results of performance evaluation

	Processing time (ns)	Number of searched combinations	System throughput (Mbps/REG[a])
w/ acceleration (Proposed)	10	100 000	64
w/o acceleration	596	1679	37

a. resource element groups.

IV. Summary

In this paper, we proposed a hardware acceleration technique that accelerates the search process in the scheduling of ultra-high-density distributed antenna systems. Our technique consists of parallel processing for calculating the throughputs of each UE simultaneously and pipeline processing for obtaining the system throughput for combinations at every clock cycle. As a result, it performs the search process 60 times faster than processing without acceleration. The proposed technique enables the scheduler to increases the number of searched combinations. The scheduling with the proposed technique enables a practical 5G system.

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References

[1] 3GPP TS36.300 “Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Universal Terrestrial Radio Access Network (E-UTRAN): Overall Description.” V13.3.0, April 2016.

[2] NTT DOCOMO, “DOCOMO 5G White Paper, 5G Radio Access: Requirements, Concept and Technologies,” White Paper, Jul. 2014.

[3] 3GPP TS36.321 “Medium Access Control (MAC) protocol specification,” V12.5.0, March 2015.

[4] Y. Arikawa *et al*., “Practical Resource Scheduling in Massive-cell Deployment for 5G Mobile Communications Systems,” International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), pp. 456-461, 9-12 Nov. 2015.

[5] ICT-317669 METIS project, “Simulation guidelines,” Del. D6.1, Oct.2013, https://www.metis2020.com/documents/deliverables/.METIS