Color Balancing-aware Non-Stitch Routing for Multiple Patterning Lithography

Jia-Hong Chang and Shao-Yun Fang
Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan
e-mail: m10607439@mail.ntust.edu.tw, syfang@mail.ntust.edu.tw

***Abstract*—Multiple Patterning Lithography (MPL) is one of the major resolution enhancement technologies for sub-20 nm nodes, which requires to decompose a layout into multiple masks considering the minimum mask spacing rule. In this paper, we propose an MPL-aware routing algorithm considering mask usage balancing to optimize pattern printability. Different from previous works, stitch insertion is not considered in our router since stitches are usually forbidden in industry to guarantee sufficient yield. To maximize the flexibility in mask usage optimization that is deficient for non-stitch routing, a multiple-objective minimum spanning tree algorithm (MO-MST) is proposed to make the distribution of generated wire segments more scattered. An integer linear programming (ILP)-based color refinement approach is also proposed to optimize mask usage balancing. Experimental results show that the proposed algorithm flow can generate MPL-compliant routing solutions with excellent mask usage balancing for the benchmarks released by 2018 CAD Contest at ICCAD.**

I. Introduction

On design for manufacturability in the advanced process nodes, lithography becomes one of the most challenging steps because of continuously shrinking features sizes. Many resolution enhancement techniques are thus proposed to enhance pattern printability such as optical proximity correction (OPC) and multiple patterning lithography (MPL). Due to the immature development of next geration lithography technologies such as extreme ultraviolet (EUV) lithography and multiple electron beam lithography (MEBL), MPL are still the major technologies adopted in industry in sub-20 nm technology nodes. In MPL, a layout is decomposed into multiple masks such that the patterns on the same mask satisfy the minimum mask spacing rule. The two most common MPL approaches are double patterning lithography (DPL) and triple patterning lithography (TPL). As shown in Fig. 1(a), if the distance between two features is smaller than the minimum mask spacing rule, the printed features would be distorted because of light diffraction. In contrast, by using two masks to print these dense features, much better pattern printability can be derived, as shown in Fig. 1(b), where the two colors represent the two different masks.

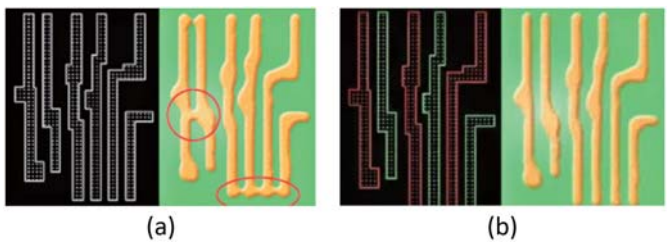

Fig. 1. The lithography results by using (a) conventional single patterning lithography and (b) double patterning lithography [1].

This work was partially supported by Synopsys, TSMC, and MOST of Taiwan under Grant No's MOST 108-2636-E-011-002.

The layout decomposition problem is usually transformed into a graph coloring problem, and thus mask assignment is often referred to as color assignment in the literature. For example, the layout decomposition problem in DPL can be modeled as a two-color assignment problem, and that in TPL is modeled as a three-coloring problem. As shown in Fig 1, each feature is assigned to either of the two colors (red or green), and the distance between two features in the same color must be larger than the minimum mask spacing. Nevertheless, a color conflict could be easily generated. As shown in Fig 2(a), there are three features A, B, C that are all within the minimum mask spacing and thus need to be assigned to different colors. Since there are only two available masks in DPL, at least one coloring conflict will be caused among these three features. To resolve coloring conflicts, stitch insertion is often adopted, which divides a single feature into few parts and assigns them into different masks. Fig. 2(b) shows that a stitch is inserted on the feature. Many previous works adopt the stitch insertion technique to resolve as many coloring conflicts as possible.

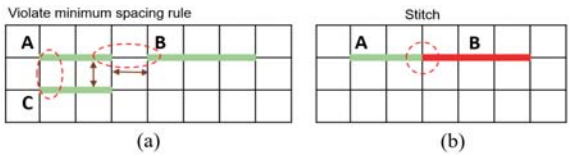

Fig. 2. A color conflict example. (a) Two conflicts in the layout (A to C and A to B). (b) A stitch is inserted on a layout feature.

On the other hand, mask usage balancing is another important issue during layout decomposition for MPL; that is, mask density uniformity should be optimized to further improve pattern resolution. Most of previous works consider mask usage balancing optimization in the post-layout optimization stage [2], [3], [4], [5], [6], [7]. They consider mask balancing either during layout decomposition or assume a decomposed result, which suffers from low optimization flexibility due to the given fixed layout.

MPL-aware design methodologies are required to provide more flexibility for MPL-related optimization. Some previous works consider layout decomposition in the detailed routing stage for DPL [8], [9], [10], [11] and TPL [12], [13], [14], while the mask usage balancing problem is rarely considered. Lei et al. proposed the first work on DPL-aware detailed routing considering mask usage balancing [11]. In their work, routing grids are first constructed and the color of each track is pre-assigned. Then, the colors of pins are determined and a 2-dimensional maze routing is used to minimize the number of stitches. Nevertheless, since stitch insertion may make patterns sensitive to overlay error and thus lead to yield loss, stitches are usually forbidden in industry. Without using stitches, the flexibility in optimizing mask usage balancing could degrade significantly.

In this paper, we propose a color balancing-aware non-stitch router for general MPL. Considering sufficient layout regularity and manufacturability required in advanced process nodes, 1-

dimensional routing is performed and stitches are forbidden. Considering the non-stitch wire structure, a multi-objective minimum spanning tree (MO-MST) is proposed to divide multi-pin nets into two-pin nets, which increases the number of groups of wire segments and thus successfully enhances the flexibility in optimizing color balancing. In addition, an integer linear programming (ILP)-based method is proposed to refine wire segment colors. Experimental results show that the proposed flow achieves superior color balancing routing results both for DPL and TPL for the benchmarks released by 2018 CAD Contest at ICCAD.

The rest of this paper is organized as follows. Section II formulates the color balancing-aware routing problem for MPL. Section III presents our proposed algorithm flow. Finally, Section IV reports the experimental results and Section V concludes the entire work.

II. Problem Formulation

Before introducing our problem formulations, some terminologies are formally defined as follows:

Definition 1: **Layer**: A layer is an available routing plane. Four layers are available in the benchmarks used in the experiments.

Definition 2: **Blockage**: A blockage is a rectangular object on a layer. Wires cannot route on blockages and must keep a minimum spacing from blockages.

Definition 3: **Via**: A via is a vertical path connecting two net shapes on adjacent layers.

Definition 4: **Wire segment**: A one-dimensional metal segment on a specific routing layer.

Definition 5: **Net**: A net connecting a set of net pins can be constructed by a set of horizontal and vertical wire segments and a set of vias among available layers.

Based on the above terminologies, the color balancing-aware routing problem can be formulated as follows:

Problem 1: **Color Balancing-aware Routing for Multiple Patterning Lithography:** Given a set of nets, the number of available layers, and the number of available masks, perform detailed routing such that the resulting layout are decomposable with m masks, and the total wirelength, the number of vias and the difference in mask usage are minimized.

III. Algorithm

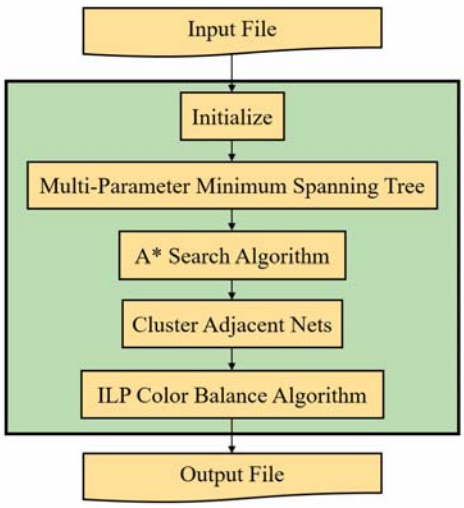

Fig. 3. The overall algorithm flow.

A non-stitch MPL-aware router should generate a routing result where the discrete pins of each net are connected by a set of horizontal segments, vertical segments, and vias without intersecting with blockages, and the wire segments on each layer should be decomposable and thus MPL-compliant. Different connection topologies for a net could result in significantly different connection costs and different impacts on mask usage balancing, which is the major challenge and optimization objective of the router. The proposed algorithm flow is shown in Fig. 3, which is composed of three stages: 1) detailed routing with multi-objective minimum spanning tree (MO-MST), 2) adjacent wire segment clustering, and 3) color balancing-aware mask assignment. MO-MST focuses on multi-pin net decomposition considering mask usage balancing before detailed routing (Section III-A). Adjacent wire segment clustering groups adjacent segments within the minimum coloring spacing into connected components (Section III-B). Finally, color-balancing-aware mask assignment optimally determines the mask assignment of each wire segment such that the difference in mask usage is minimized (Section III-C). We detailed the three steps in the following subsections.

A. Detailed Routing Multi-Objective Minimum Spanning Tree (MO-MST)

In the first stage, detailed routing is performed to simultaneously minimize the connection cost (wirelength and the number of vias) and optimize the flexibility in mask usage balancing. Our idea is to increase the number of wire segment groups in a generated routing result, and thus larger solution space can be provided for the final ILP-based color refinement stage. A wire segment group is a single connected component in the conflict graph, whose color assignment is independent of other wire segment groups.

Before detailed routing with conventional path searching methods, a multi-pin net needs to be decomposed into a set of two-pin nets, which is usually achieved by first constructing a spanning graph, where each vertex represents a pin of the net, and the weight of each edge connecting a pair of pins indicates the connection cost of the two pins. Then, a minimum spanning tree is found on the graph, whose composing edges are the 2-pin nets minimizing the total connection cost. To consider mask usage balancing at the same time, we modify the edge cost setting of the spanning graph to generate a multi-objective minimum spanning tree (MO-MST), and thus a better trade-off between the connection cost and color balancing can be achieved. The weight of each edge can be computed as follows:

$$w(e) = \alpha \times M + \beta \times P + \gamma \times B, \tag{1}$$

where α, β and γ are three user-specified parameters, M denotes the Manhattan distance of the two pins, P denotes the number of other pins adjacent to the bounding box of the two pins, and B is the number of blockage grids in the bounding box. Fig. 4 gives an instance of the edge weight computation approach, where M, P, and B are 12, 2, and 9, separately.

It is intuitive that larger M and B are usually result in a larger connection cost. The cost setting also takes P into account, as larger P may reduce the number of wire segment groups during detailed routing. Fig. 5 shows an example, where a 3-pin (green pins in Fig. 5) net is divided into two 2-pin nets. Without considering the pin cost, the two 2-pin nets would be ab and ac as the three edges have the same connection cost and the corresponding three-dimensional wiring layout is shown in Fig. 5(a), where three wire segment groups are generated. By considering the pin cost, in contrast, the two 2-pin nets become ab and bc. It can be observed that the wire segments become more scattered, and thus more wire segment groups are generated, as illustrated in Fig. 5(b).

Having a set of 2-pin nets, the A*-search algorithm is adopted for detailed routing. In this stage, the objective is to guarantee the decomposability of the resulting wire segments, and thus track precoloring is first applied [11], and each wire segment is assigned a

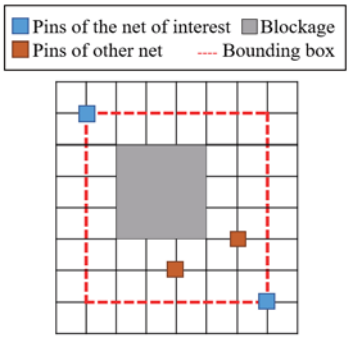

Fig. 4. For the edge weight computation of the two blue pins, M, P, and B in Equation (1) are 12, 2, and 9, separately.

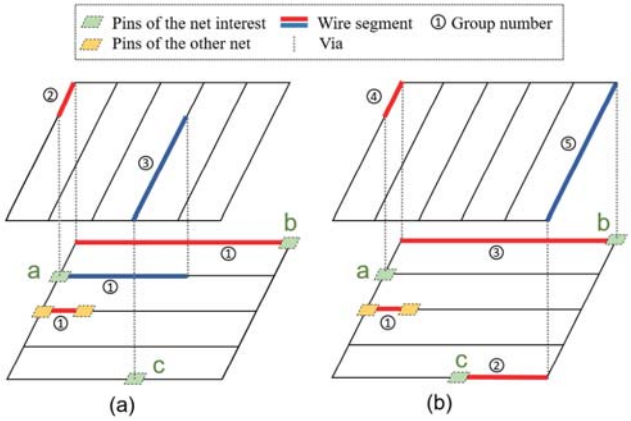

Fig. 5. (a) The MST derived without considering the pin cost and three wire segment groups are generated for the MST (b) The MO-MST derived by considering the pin cost and five wire segment groups are generated for the MO-MST.

color according to its corresponding track. Fig. 6 shows an example of track pre-coloring for DPL. The A*-search algorithm stops searching once a routing grid occupied by the same net is reached, which may cause shorter wirelength with a Steiner tree topology.

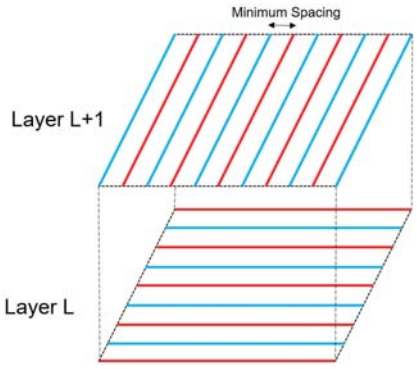

Fig. 6. The 1D routing grid is assigned the color by our method. The smallest distance between the same color tracks is 2 times minimum spacing.

B. Adjacent Wire Segment Clustering

Having a detailed routing result, the layout decomposability of the wire segments on each layout is guaranteed and each wire segment is pre-assigned to a mask according to the track it belongs to. However, the mask assignment result is not necessarily the one minimizing the difference in mask usage among different masks. Based on the assumption that a layout is decomposable, Chen et al. showed that by using *the color rotation technique*, color balancing can be further improved [7]. Color rotation rotates the colors of the wire segments in a connected component. For example, by exchanging the mask assignment of the wire segments in a connected component in DPL, the difference in mask usage of the two masks may be reduced. To utilize the color rotation technique, connected components need to be first identified.

We propose an efficient method to cluster all adjacent wire segments into a connected component. The proposed method takes only linear time with respect to the total number of wire segments on each layer. The idea of net clustering is based on segment propagation on a plane, which is demonstrated in Figs. 7 and 8. Given a wire segment, s, we recursively find its its adjacent wire segments and cluster them into a group. We keep traversing unclustered segments until all wire segments are grouped into components components.

Algorithm: Adjacent Segment Clustering
Input: S_l: a set of wire segments on layer l
Goal: Determine the group index of each wire segment
1 $i \leftarrow 0$
2 **for** $\forall s \in S_l$
3 $i \leftarrow i + 1$
4 **if** $s.group = \phi$
5 $s.group \leftarrow i$
6 $FindNeighbors(s, i)$
7 **end if**
8 **end for**

Fig. 7. The algorithm used to cluster all adjacent nets.

Procedure: $FindNeighbors(s, i)$
1 $\forall s_{adj}$ adjacent to s
2 **if** $s_{adj}.group = \phi$
3 $s_{adj}.group \leftarrow i$
4 $FindNeighbors(s_{adj}, i)$

Fig. 8. The algorithm used to find all neighbors.

C. Color Balancing-aware Mask Assignment Refinement

After identifying all connected components with their coloring results, the last step is to utilize the color rotation technique to further refine mask usage balancing. Due to the pin cost consideration during MO-MST, many wire segment components can be derived on each layer, and thus there could be much room for improvement in color balancing. The color ratio scoring method in 2018 CAD Contest at ICCAD is as follows:

$$min \quad |\frac{\sum_{l=1}^{L} N_{m_1}^l}{\sum_{l=1}^{L} T_l} - 0.5| \tag{2}$$

where $N_{m_1}^l$ is the total length of wires assigned to Mask 1 on Layer l, and T_l is the total wirelength on Layer l. To optimize the color ratio, we propose an ILP-based method to refine the color

TABLE III
THE EXPERIMENTAL RESULTS FOR TPL. M1, M2, M3 DENOTE THE MASK1, MASK2 AND MASK3, RESPECTIVELY.

Benchmark	WL	Color Ratio (%)						Runtime (s)	
		w/o ILP			w/ ILP			w/o ILP	w/ ILP
		M1 (%)	M2 (%)	M3 (%)	M1 (%)	M2 (%)	M3 (%)	(s)	(s)
Case 1	5185.5	29.795	33.690	36.515	33.333	33.333	33.333	0.176	0.378
Case 2	9478	31.895	35.366	32.739	33.329	33.335	33.335	0.297	0.480
Case 3	10294	29.051	37.012	33.93	33.330	33.335	33.335	0.324	0.555
Average	-	30.247	35.356	34.397	33.330	33.334	33.334	-	-

assignment of each wire segment group for optimizing mask usage balancing.

The notations used in the ILP formulation are listed as follows:

- g: the number of wire segment groups.
- m: the number of available masks.
- T: the total wirelength of the routing result.
- $N^i_{M_j}$: the total wirelength of the wire segments of Group i assigned to Mask j in the original detailed routing result.
- M^i_j: a Boolean variable, $M^i_j = 1$ means that the wire segments of Group i assigned to Mask j in the original detailed routing result are reassigned to the target mask.

With the notations, the ILP formulation is as follows:

$$\min \quad \sum_{i=1}^{g}\sum_{j=1}^{m} M^i_j \times N^i_{M_j} \tag{3}$$

$$s.t. \quad \sum_{i=1}^{g}\sum_{j=1}^{m} M^i_j \times N^i_{M_j} \geq \frac{T}{m} \tag{4}$$

$$\sum_{j=1}^{m} M^i_j = 1 \ \forall\, g \in group \tag{5}$$

This formulation tries to find a set of wire segments for each group, which are assigned to the same mask in the original routing result, such that the total wirelength of the selected segments approaches the target mask usage. For DPL, $m = 2$ and thus the target mask usage is 50% of the total wirelength (T). For TPL, $m = 3$ such that the target mask usage is about 33% of T.

IV. EXPERIMENTAL RESULTS

We implemented our algorithm flow with the C++ programming language and all experiments were performed on a 3.5 GHz Linux machine with 72 GB memory. The CPLEX optimizer is employed as our ILP solver [15]. The benchmarks were obtained from

TABLE I
THE BENCHMARK STATISTICS.

Benchmark	PIN	NET
Case 1	100	33
Case 2	140	68
Case 3	152	72

the Domestic 2018 CAD Contest at ICCAD. Table I lists the detailed information of each benchmark circuit. The user-specified parameters are set as α=0.5, β=0.5, and γ=0.5 in our experiment. The experimental results for DPL and TPL are respectively shown in Table II and III, where total wirelength, the number of vias and the color usage ratio are reported. It is worth to note that the color usage ratio results almost achieve optimal solutions for every case.

TABLE II
THE EXPERIMENTAL RESULTS FOR DPL. WL, VIA DENOTE THE WIRELENGTH, THE NUMBER OF VIA. W/O ILP AND W/ ILP DENOTE WITHOUT AND WITH ILP-SOLVER.

Benchmark	WL	Via	Color Ratio (%)		Runtime (s)	
			w/o ILP	w/ ILP	w/o ILP	w/ ILP
Case 1	5185.5	177	77.880	49.995	0.179	0.295
Case 2	9478	243	55.877	50.0	0.298	0.392
Case 3	10294	287	53.779	50.0	0.316	0.431
Average	-	-	62.512	49.998	0.264	0.373

V. CONCLUSION

In this paper, we propose a non-stitch MPL-aware router considering mask usage balancing. Based on the idea that more connected components of wire segments can provide more flexibility of color balancing optimization, an MO-MST algorithm is proposed to decompose multi-pin nets into 2-pin nets. Having the detailed routing result, an ILP formulation is to refine the color usage ratio. Experimental results show that our algorithm flow can achieve nearly optimal color usage ratios both for DPL and TPL on the benchmarks provided by 2018 CAD Contest at ICCAD.

REFERENCES

[1] https://www.quora.com/What-is-double-patterning-in-VLSI
[2] J. Kuang, and E. F. Y. Young, "An efficient layout decomposition approach for triple patterning lithography," *Proc. DAC*, pp. 1–6, 2013.
[3] Y. Zhang, W.-S. Luk, H. Zhou, C. Yan, and X. Zeng, "Layout decomposition with pairwise coloring for multiple patterning lithography," *Proc. ICCAD*, pp. 170–177, 2013.
[4] Shao-Yun Fang, Yao-Wen Chang, Wei-Yu Chen "A novel layout decomposition algorithm for triple patterning lithography," *Proc. DAC*, pp. 1181–1186, 2012.
[5] K. Yuan, J.-S. Yang, and D. Z. Pan, "Double patterning layout decomposition for simultaneous conflict and stitch minimization," *Proc. IEEE TCAD*, pp. 185–196, 2010.
[6] B. Yu, K. Yuan, B. Zhang, D. Ding, and D. Z. Pan, "Layout decomposition for triple patterning lithography," *Proc. IEEE TCAD*, pp. 433–446, 2015.
[7] Kuan-Jung Chen, Shao-Yun Fang, "Printability Enhancement with Color Balancing for Multiple Patterning Lithography," *Proc. IEEE TETC*, pp. 1–1, 2018.
[8] M. Cho, Y. Ban and D. Z. Pan, "Double patterning technology friendly detailed routing," *Proc. ICCAD*, pp. 506–511, 2008.
[9] X. Gao and L. Macchiarulo, "Enhancing double-patterning detailed routing with lazy coloring and within-path conflict avoidance," *Proc. DATE*, pp. 1279–1284, 2010.
[10] I. Abed and A. G. Wassal, "Double-patterning friendly gridbased detailed routing with online conflict resolution," *Proc. DATE*, pp. 1475–1478, 2012.
[11] Seong-I Lei, Chris Chu, and Wai-Kei Mak, "Double Patterning-Aware Detailed Routing with Mask Usage Balancing," *Proc. ISQED*, pp. 219–223, 2014.
[12] B. Yu, Y.-H. Lin, G. Luk-Pat, D. Ding, K. Lucas, and D. Z. Pan, "A high-performance triple patterning layout decomposer with balanced density," *Proc. ICCAD*, pp. 163–169, 2013.
[13] Hua-Yi Wu, Shao-Yun Fang, "Triple Patterning Lithography-aware Detailed Routing Ensuring Via Layer Decomposability," *Proc. VLSI-DAT*, pp. 1–4, 2018.
[14] P. Y. Hsu, and Y. W Chang, "Non-stitch triple patterning-aware routing based on conflict graph pre-coloring," *Proc. ASP-DAC*, pp. 390–395, 2015.
[15] IBM ILOG CPLEX Optimizer. https://www.ibm.com/analytics/cplex-optimizer