Test Plan For Detecting Mersenne Twister Faults In BIST

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Abstract— Mersenne twister can be utilized to generate test patterns for detecting LSI faults. The utilization of the Mersenne twister as a test pattern generator can improve the fault coverage. However, the Mersenne Twister may contain faults. Therefore, this paper examines whether there is a test sequence for detecting the Mersenne Twister faults. Experimental results show that the Mersenne Twister has a test sequence that reaches a 100% fault coverage for stuck-at faults.

I. INTRODUCTION

Nowadays, the scale and performance of LSIs are increasing along with the miniaturization of semiconductor processes. On the other hand, testing of LSIs has become difficult. Therefore, a test method for the efficient detection of LSI fault is needed.

Manufacturing tests are performed using the tester. The tester applies the test patterns to the LSI. The tester is very expensive, and occupying a tester during testing increases the cost of testing. A solution to this problem is the built-in self test (BIST), in which a part of the tester function is built into the LSI. BIST tests by applying a test pattern from the Test Pattern Generator (TPG) to the circuit under test. There is a method of utilizing pseudo-random numbers as a test pattern generator. The Linear Feed-Forward Shift Register(LF^2SR) and Linear Feedback Shift Registers(LFSR) are mainly utilized to generate pseudo-random numbers. The LF^2SR and LFSR have a small increase in area as a test pattern generator. However, high fault coverage cannot be achieved for sequential circuits. Another way to generate pseudo-random numbers is to utilize the Mersenne Twister [3] as a test pattern. The Mersenne Twister has a very long period (2^{19937}- 1) and high randomness, such that the correlation between the values is negligible. Therefore, it has been shown that the Mersenne Twister obtains the high fault coverage for sequential circuits [1].

However, the hardware conversion of the Mersenne twister may contain defects. If the Mersenne Twister fail, it may mask the faults in the circuit under test. If the faults are masked, the fault coverage will increase. Therefore, it is necessary to consider the test of the Mersenne Twister. It has been proved in [4] that there exists a test sequence to detect stuck-at faults for the LF^2SR and LFSR. Since a test sequence exists for the LF^2SR and LFSR, there may be a test sequence for the Mersenne Twister that reaches a 100% fault coverage. In this paper, we show that there exists a test sequence for the Mersenne Twister.

II. METHOD

There are several versions of the Mersenne Twister. In this paper, we chose the generally used generation method, MT19937 [3]. MT19937 has a very long period of 2^{19937}- 1. Also, it has been mathematically proven that the Mersenne Twister is evenly distributed in higher dimensions (623 dimensions). Therefore, the correlation between successive values in the output is negligible. The Mersenne Twister to which a continuous pattern can be applied is shown in [2]. Figure II shows one way to implement MT19937 in hardware.

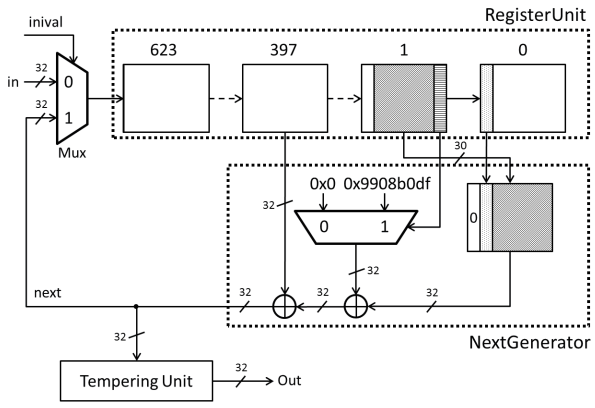

Fig. 1. An example of Hardware structure of MT19937

The circuit is constructed from three units, "Register Unit", "Next Generator Unit" and "Tempering Unit". "Register Unit" is a group of registers that holds the internal state of the device. At each rising or negative clock edge, the value held in the register is shifted to the next register. "Next Generator Unit" is the main part

of the pseudo-random number generator. It performs a shift operation on the input and performs an exclusive OR. When generating pseudo-random numbers, 3 specific words (words 0,1,397) out of 624 words are utilized. "Tempering Unit" is the circuit to improve the variance of the output pseudo-random number sequence. The input and output signals of the circuit are shown in Table I. In Table I, While inival is 0, the rising or negative clock edge applies an initial state to the register from the external input "in". While inival is 1, the feedback value is applied to the register at the rising or negative clock edge.

TABLE I
THE INPUT AND OUTPUT SIGNALS OF MT19937

Signal name	Input or Output	Number of bits
in	Input	32
inival	Input	1
clock	Input	1
reset	Input	1
out	Output	32

We designed the Mersenne Twister in Verilog HDL based on Figure II. We utilized Synopsys design compiler to perform the logic synthesis of the Mersenne Twister. The fault coverage is obtained by performing the fault simulation of the TetraMAX tool. The fault simulation is based on the test plan. The test plan is set up to control the external input to increase the fault coverage. The test plan is shown in the Table II.

TABLE II
THE TEST PLAN OF THE MERSENNE TWISTER

Signal name		
reset	inival	number of clock cycles
1	1	624
0	1	624
0	0	232

Since the register of the "Register Unit" is initially set to the undefined value, during the first 624 clocks, initialize the registers in the "Register Unit" of the Mersenne Twister by setting reset to 1. The initialization applies 0 from the input for 624 clocks to set 0 to all registers of the "Register Unit". Next, to apply the initial status to the register of "Register Unit", the signal changes the reset to 1 and applies the value to the register from the external input "in". In this paper, random patterns are applied to all registers of the "Register Unit" as an initial state. Finally, during the 232 clocks, the signal changes the inival to 0. Therefore, a random number generated from the initial state of the register is applied to the register.

III. Evaluation Experiment

The results of the fault simulation by TetraMax are shown in Table III.

TABLE III
REPORT_FAULTS WHEN A FAULT IS APPLIED TO THE ENTIRE CIRCUIT

fault class	#faults
Detected	120,741
Possibly detected	3
Not detected	0
total faults	120,744
fault coverage	100%

The total faults were 120,744, detected faults were 120,741, and possibly detected were 3, as shown in Table III. Therefore, the fault coverage is 100%, as shown in Table III. The possibly detected faults are the reset signals. Possibly detected is a fault that may have been detected by the fault simulation. Therefore, we consider that possibly detected is the detectable fault. Experimental results show that a 100% fault coverage of the Mersenne Twister can be achieved by utilizing a random pattern. The minimum number of clock cycles in the test plan to achieve a 100% fault coverage was found.

IV. Conclusion

In this paper, we applied a random sequence to the Mersenne twister. A test plan was created and the fault simulation was performed based on the test plan. Experimental results show that there is a test sequence for the Mersenne Twister with a 100% fault coverage for stuck-at faults. Therefore, we show that it is possible to detect stuck-at faults of the Mersenne Twister. The future plan is to establish a test methodology for Mersenne twister. For that purpose, we will prove a test sequence for each fault.

References

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