# A Transimpedance Amplifier Topology Considering the Impact of Variability on Inductive Peaking

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**Abstract— This paper proposes a transimpedance amplifier topology for reducing the impact of parasitic inductance and the variability of poly-resistors. When inductive peaking is used, parasitic inductance and variability cause over-peaking. We propose a circuit topology that the dumping factor increases as the parasitic inductance increases. Also, the proposed topology is tolerant against the variability of the poly-resistors. Simulation results show the proposed circuit realizes 74% larger eye-opening compared to the conventional topology.**

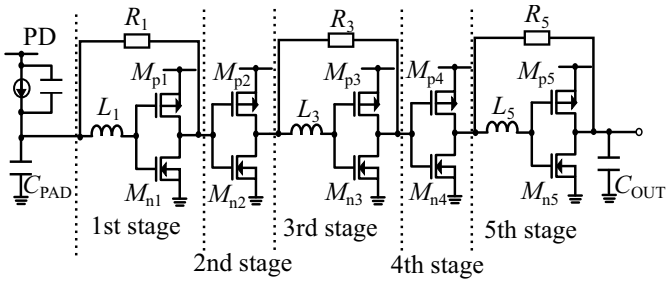



Fig. 1. Schematic of the reference TIA.

## I. Introduction

Optical communication system is one of the important technologies for high capacity data transfer[1]. High bandwidth of transimpedance amplifier (TIA) is needed to improve the transfer rate. Inductive peaking is widely used to achieve high bandwidth[2]. Too much inductive peaking is called over-peaking. Over-peaking causes overshoot/undershoot and larger jitter due to the group delay deviation. On the other hand, under-peaking cannot enhance bandwidth. Thus, adequate peaking is required for high performance TIA. However, inductive peaking is affected by parasitic inductance and variability. The interconnects among inductors and other circuit components have parasitic inductance[3]. As the operating speed becomes higher, the inductance value for inductive peaking becomes small. Then, the impact of the parasitic inductance becomes relatively larger. Also, the poly-resistor often varies with decreasing resistance[4]. These factors are difficult to compensate for after fabrication. Thus, parasitic inductance and variability are a serious issue for inductive peaking. Additionally, parallel integration of multiple channels is a common way for higher data capacity. In such cases, inter-channel variation might cause performance degradation. Thus variability-tolerant is important in multi-channel optical receiver chips.

This paper discusses the impact of parasitic inductance and variability on inductive peaking. We employ a five-stage inverter-type TIA with three inductors[5] as the reference topology. The reference circuit includes three poly-resistors to determine the transimpedance gain. The goal of this work is to prevent the impact of the parasitic inductance and the variability of the inductive peaking. The parasitic inductance and the decrease of the resistance cause over-peaking because the dumping factor of inductors decreases. We modify the 3rd stage of the reference circuit and the proposed topology has less sensitivity to the parasitic inductance and the resistance variation.

We simulated a 30 Gb/s TIA in 65-nm CMOS. In the case of +20% parasitic inductance of inductor, the eye-opening area is improved by 17% compared to the reference. In the case of −20% variation of the poly-resistors, the eye-opening area is improved by 74% compared to the reference. The contribution of this paper is to clarify the impact of variability on over-peaking and to prevent the eye-diagrams degradation by over-peaking.

## II. Performance Analysis of Inverter Type TIA

In this section, we first describe the behavior of the reference and the proposed TIA. Then, we explain the impact of parasitic inductance and variability.

### A. Behavior of the Reference and the Proposed TIA

First, we explain the behavior of the reference TIA. Fig. 1 shows inverter-type TIA (INV-TIA) with peaking

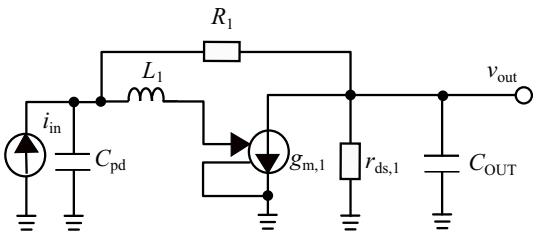



Fig. 2. The small-signal equivalent circuit of pre-amplifier in the reference.

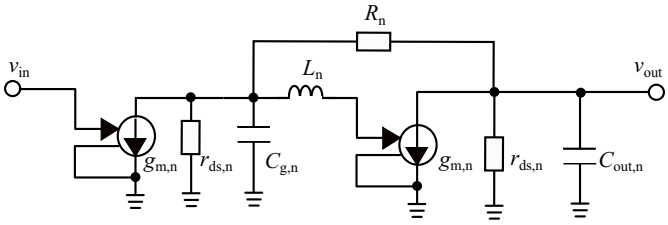



Fig. 3. The small-signal equivalent circuit of Cherry-Hooper amplifier in the reference.

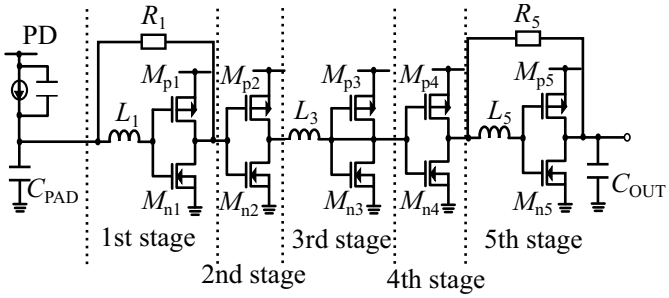



Fig. 4. Sschematic of the proposed TIA.

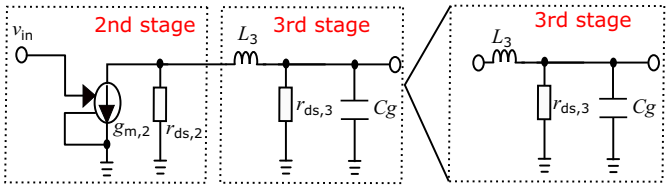



Fig. 5. The small-signal equivalent circuit of the 2nd and the 3rd stages of the proposed TIA.

inductors. The inductors for series peaking are inserted at the gate node of the 1st, the 3rd, and the 5th stages. The reference circuit has five stages and the 1st stage is the pre-amplifier, and the 2nd and the 3rd stages, the 4th and the 5th stages composes Cherry-Hooper amplifiers. Fig. 2 and Fig. 3 show simplified small-signal equivalent circuit of the pre-amplifier and the Cherry-Hooper amplifier, respectively. Here, $g_{m,n}$ is the transconductance, $r_{ds,n}$ is output resistance, $R_n$ is feedback resistance, and $n$ is the index of the stages. From Fig. 2 and Fig. 3, the transimpedance gain of the reference TIA is derived as

$$Z_{T,ref} = \frac{r_{ds,1} - A_1 R_1}{A_1 + 1} \times \frac{A_2 \left(A_3 R_3 - r_{ds,3}\right)}{R_3 + r_{ds,2} + r_{ds,3} + r_{ds,2} A_3} \times \frac{A_4 \left(A_5 R_5 - r_{ds,5}\right)}{R_5 + r_{ds,4} + r_{ds,5} + r_{ds,4} A_5}, \quad (1)$$

where $A_n$ is the voltage gain of $n$-th stage and is equal to $g_{m,n} r_{ds,n}$.

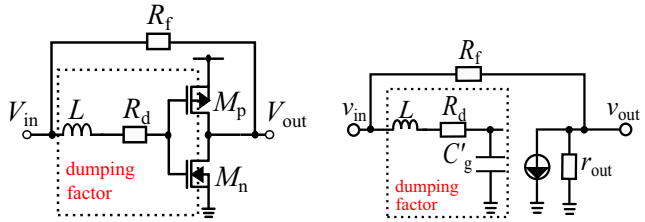
Next, we explain the behavior of the proposed TIA. Fig. 4 shows the proposed TIA. The 3rd stage of the proposed TIA is composed of a diode-connected pMOS and nMOS. Fig. 5 shows the small-signal equivalent circuit of the 2nd and the 3rd stages of the proposed TIA. Here, $g_{m,n}$ is the transconductance, $r_{ds,n}$ is output resistance, $R_n$ is feedback resistance, and $n$ is the index stage. From Fig. 2, Fig. 3, and Fig. 5, the transimpedance gain of proposed TIA is derived as

$$Z_{T,pro} = \frac{r_{ds,1} - A_1 R_1}{A_1 + 1} \times \frac{-A_2 r_{ds,3}}{r_{ds,2} + r_{ds,3} + r_{ds,2} A_3} \times \frac{A_4 \left(A_5 R_5 - r_{ds,5}\right)}{R_5 + r_{ds,4} + r_{ds,5} + r_{ds,4} A_5}, \quad (2)$$

where $A_n$ is the voltage gain of $n$-th stage and is equal to $g_{m,n} r_{ds,n}$.

### B. *Impact of Variability*

We explain the impact of variability. From Eq. (1) and Eq. (2), the transimpedance gain is deeply related to the feedback resistance. The variation of the poly-resistors changes the transimpedance gain. Change of the transimpedance gain affects inductive peaking. Here, we compare Eq. (1) and Eq. (2). From Eq. (1), transimpedance gain of the reference TIA is affected by $R_1$, $R_3$, and $R_5$. On the other hand, from Eq. (2), transimpedance gain of the proposed TIA is affected by $R_1$ and $R_5$. The resistance of the poly-resistors tends to decrease with variability. Thus, the transimpedance gain of the reference with three feedback resistors tends to decrease more than the transimpedance gain of the proposed TIA. Also, the degradation of the transimpedance gain causes over-peaking. On the other hand, the proposed TIA has one less feedback resistor than the reference, so the degradation of the transimpedance gain can be prevented. Accordingly, the proposed TIA has less impact on the variation of the poly-resistors than the reference.




(a) Schematic of INV-TIA with dumping resistor.

(b) Small-signal equivalent circuit.

Fig. 6. INV-TIA with dumping resistor.

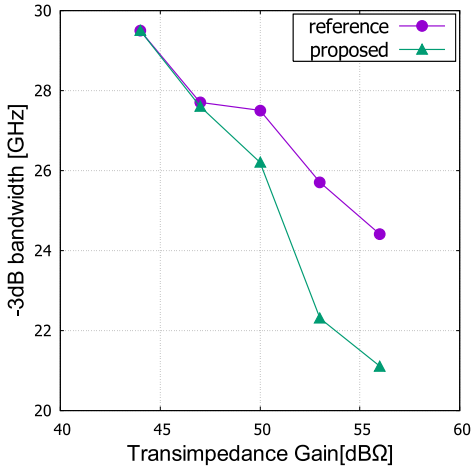



Fig. 7. Relationship between the transimpedance gain and the bandwidth.

### C. *Impact of Parasitic Inductance*

We explain the impact of the parasitic inductance. Parasitic inductance increases inductive peaking. Over-peaking causes overshoot/undershoot and larger jitter due to the group delay deviation. A dumping resistor is used to prevent the over-peaking. The dumping resistor is inserted in series with the inductor like Fig. 6(a). Here, $R_d$ is a dumping resistor and $R_f$ is a feedback reference. From Fig. 6(b), secondary transfer function $H(s)$ is derived as

$$H(s) = \frac{\frac{1}{LC'_g}}{s^2 + \frac{R_d}{L}s + \frac{1}{LC'_g}}, \tag{3}$$

here, resonant frequency $\omega_c$ is expressed by $\frac{1}{\sqrt{LC'_g}}$ and Eq. (3) is rewritten by

$$H(s) = \frac{\omega_c^2}{s^2 + \omega_c R_d \sqrt{\frac{C'_g}{L}}s + \omega_c^2}, \tag{4}$$

here, $s = j\omega$, $C'_g$ is the total capacitance of the gate node, that includes the gate capacitance $C_g$ and the gate-drain capacitance with Miller effect, and $R_d\sqrt{\frac{C'_g}{L}} = \xi$. $\xi$ is the dumping factor of INV-TIA with the dumping resistor inserted. From Eq. (4), when the parasitic inductance increases, the dumping factor becomes smaller than the situation without parasitic inductance. Decreasing dumping factor indicates that over-peaking is occurring. Thus, the method of inserting the dumping resistor causes over-peaking when the inductance increases by parasitic inductance.

In addition, from the 3rd stage of Fig. 5, secondary transfer function of the proposed TIA $H'(s)$ is derived as

$$H'(s) = \frac{\frac{1}{L_3C_g}}{s^2 + \frac{1}{r_{ds,3}C_g}s + \frac{1}{L_3C_g}}, \tag{5}$$

here, resonant frequency $\omega_c$ is expressed by $\frac{1}{\sqrt{L_3C_g}}$ and Eq. (5) is rewritten by

$$H'(s) = \frac{\omega_c^2}{s^2 + \omega_c \frac{1}{r_{ds,3}}\sqrt{\frac{L_3}{C_g}}s + \omega_c^2}, \tag{6}$$

here, $\frac{1}{r_{ds,3}}\sqrt{\frac{L_3}{C_g}} = \xi'$. $\xi'$ is the dumping factor of the 3rd stage with the proposed TIA. From Eq. (6), when the parasitic inductance increases, the dumping factor becomes larger. Increasing the dumping factor can prevent the impact on inductive peaking. Thus, the proposed TIA can prevent the impact on inductive peaking when the inductance increases by parasitic inductance.

## III. Simulation Results

This section compares the Performance of the reference and the proposed TIA. First, we reveal the relationship between the transimpedance gain and the bandwidth of the reference and the proposed TIA. Next, we illustrate the impact of parasitic inductance and variability on the eye-opening area.

### A. *Relationship Between Gain and Bandwidth*

First, we show the comparison of the gain-bandwidth relationship of the reference and the proposed TIA. From the discussion in Section II, the proposed TIA can reduce the impact of the parasitic inductance and the variability on over-peaking. On the other hand, the proposed topology degrades the bandwidth. Fig. 7 shows the simulation results. Since there is a trade-off between the gain and the bandwidth, as the transimpedance gain increases, the bandwidth decreases. From Fig. 7, the bandwidth of the proposed TIA drops rapidly as the transimpedance gain increases. This means that the proposed topology has a drawback when the required gain is high. On the other hand, when the gain is less than 50 dBΩ, the bandwidth of the proposed TIA is almost the same as that of the reference. Thus, the proposed topology is suitable for low transimpedance gain and high speed configuration.

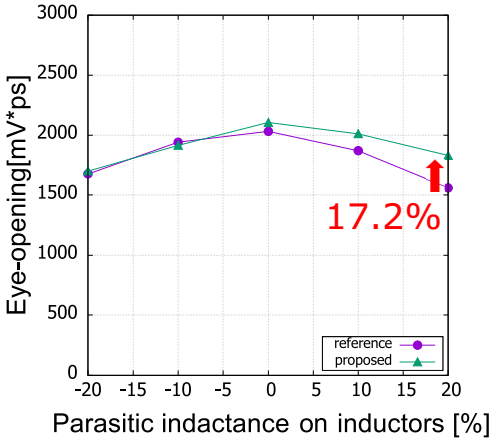
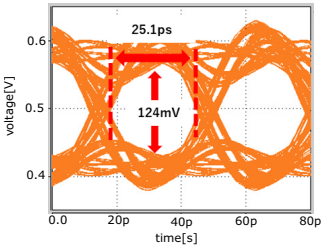
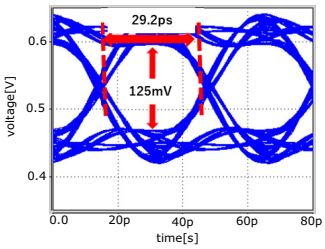



Fig. 8. Impact of the parasitic inductance on the eye-opening area.




(a) Eye-diagrams of the reference TIA.




(b) Eye-diagrams of the proposed TIA.

Fig. 9. Eye-diagrams in the case of +20% parasitic inductance.

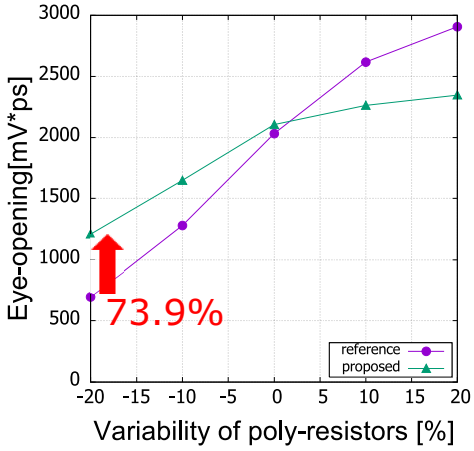
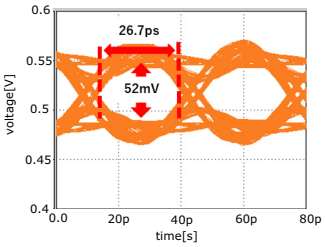
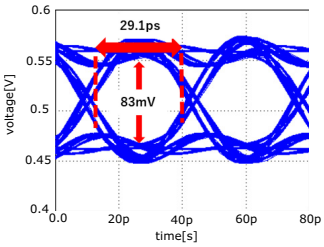



Fig. 10. Impact of the poly-resistors variation on the eye-opening area.




(a) Eye-diagrams of the reference TIA.




(b) Eye-diagrams of the proposed TIA.

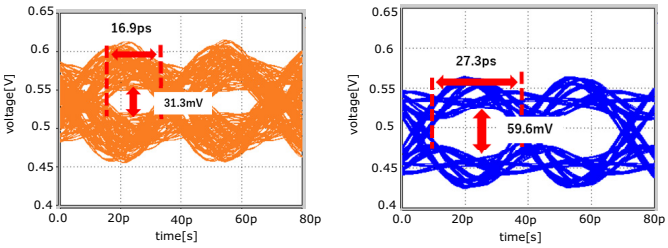
Fig. 11. Eye-diagrams in the case of −20% variation of the poly-resistors.

### B. *Relationship Between Parasitic Inductance of Inductor and Eye-Opening Area*

We describe the impact of parasitic inductance on the eye-opening area. Over-peaking causes overshoot/undershoot and jitter due to the group delay deviation. Thus, we use the eye-opening area as the measure of performance. We define the eye-opening area by the product of the maximum eye-opening voltage and the maximum eye-opening period. The transimpedance gain is set to 50 dBΩ, and we evaluate the eye-opening area with 30 Gb/s PRBS input by a transistor-level circuit simulation. Fig. 8 shows the relationship between the parasitic inductance on the inductors and the eye-opening area. Since the circuit is designed assuming 0% parasitic inductance, the eye-opening area becomes maximum at the parasitic inductance is 0%. As the parasitic inductance increases, the eye-opening area degrades. From Fig. 8, the degradation of the proposed TIA is smaller than the reference TIA. When the parasitic inductance is +20%, the proposed TIA achieves 17% larger eye-opening area. Fig. 9 shows the eye-diagrams at +20% parasitic inductance. The eye-opening voltages are almost the same. However in the reference TIA, the jitter increases and the eye-opening width is 25.1 ps although the proposed TIA obtains 29.2 ps width.

### C. *Relationship Between Variation of the Poly-Resistors and Eye-Opening Area*

Next, we evaluate the impact of the variability of the poly-resistors. When the resistance becomes smaller by variation, the transimpedance gain becomes smaller and the inductive peaking becomes too strong. Fig. 10 shows the relationship between the variation and the eye-opening area. When the resistances decrease by the variation, the transimpedance gain decreases, and the jitter increases by over-peaking. As shown in Fig. 10, the degradation of the eye-opening of the proposed TIA is gentler than that of the reference TIA. In the case of −20% variation, the proposed TIA achieves a 74% larger eye-opening area. Fig. 11 shows the eye-diagrams at −20% variation. The proposed TIA keeps both larger eye-opening voltage and smaller jitter. The eye-opening voltage is 60% larger and the eye-opening width is 9% larger.




(a) Eye-diagrams of the reference TIA.

(b) Eye-diagrams of the proposed TIA.

Fig. 12. Eye-diagrams in the case of the MOS is varied.

### D. *Relationship Between Variation of the MOS and Eye-Opening Area*

As the parasitic inductance on the inductors and the variability of the poly-resistors, the variation of MOS transistors should be considered. Here, we examine the impact of MOS variation. Since over-peaking occurs when the MOS transistors varied toward the "fast" side, Fig. 12 shows the eye-diagrams when all MOS transistors are set to FF (Fast-Fast) condition. From Fig. 12, the proposed TIA achieves a 207% larger eye-opening area. The eye-opening voltage is 90% larger and the eye-opening width is 61% larger. From the discussion above, the proposed TIA is more tolerant against the parasitic inductance on the inductors, the variation of the poly-resistor, and the variation of the MOS transistors.

## IV. Conclusion

This paper proposes a transimpedance amplifier topology that is tolerant against variabilities. Transimpedance amplifiers with inductive peaking suffer from over-peaking caused by variability and parasitic inductance. The proposed topology is a modified inverter-type TIA. By using the differential resistances of diode-connected MOS transistors, we invert the impact of the parasitic inductance and the variability on the dumping factor. Simulation results show that the proposed TIA achieves a larger eye-opening area with the parasitic inductance and the variability. Since it is difficult to compensate for the over-peaking after fabrication, the proposed topology is effective to realize high speed TIA.

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