Power Domain Layer Assignment in Package Substrate Design

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Abstract— With the increasing functional integration in modern integrated circuits, both the chip size and design complexity are inevitably increasing. In addition, the number of power domains is drastically increased owing to the demands of power efficiency in various functional modules. Thus, reliable power delivery has become one critical issue in package substrate design. In this paper, we are the first work to automate power domain layer assignment in package substrate design. First, seed selection step selects critical power domains with larger area conflict and assigns these critical domains to separated metal layers. After that, remaining power domains are assigned to proper metal layers taking power pin distribution into account. Experimental results demonstrate the effectiveness of our layer assignment algorithm for the follow-up polygon layout partition.

I. Introduction

Due to the rapid of the development in big data, artificial intelligence, 5G Internet of things, etc., the demand for the chip technology is getting higher, and the packaging technology for system-level integration has become an important trend.

AMD combines heterogeneous 7nm CPU with 10nm I/O using package level integration on the same package substrate to improve system yield. [1] Besides making the smaller and more efficient chip, the integration of packaging technology is also a major direction in the future. From the pin through hole (PTH), surface mount technology (SMT), ball grid array package (BGA). Up to now, flip chip package (FCP), wire bonding package and many advanced packaging technologies such as flip-chip packaging, fan-out packaging (FO), wafer level packaging (WLP), 2.5D/3D packaging, heterogeneous integrated packaging and targeting for 5G Antenna in Package (AiP). [2] $\sim$ [7] The evolution of packaging technology enables the electronic products greater progress. Packaging is important in the electronic products to protect the chip from external physical and chemical materials, to provide chip signal insulation protection, to avoid signal mutual interference, and attenuation, to provide heat dissipation channel and improve handling.

In this paper, we focus on the substrate power delivery in both flip-chip package and wire-bond package. With the advancement of modern low-power design technology, the requirements of various voltage domains under crucial current and quality constraints are drastically increasing. The substrate must provide power distribution, signal distribution and provide a stable platform enough to that of the mounted components to be reliable over many thermal cycles. [8] If the various power domains are too close, the performance and power integrity will be affected. [9] Therefore, planning substrate power domains is a critical challenge in modern package design. This motivates us to develop a design automation methodology for power domain planning.

The rest of this paper is organized as follows. Section II is to talk about our motivation and purpose of the Power Domain Layer Assignment. Section III gives the overview of our definition and motivation. Section IV introduce how our algorithm works. The experimental results are drawn in Section V. Finally, Section VI concludes our work.

II. Preliminary

A. Motivation

As the chip size and design complexity increases, the power demand is becoming huge. In recent years, multiple power domain design complicates the power delivery problem within a package substrate. Since each individual power domain requires different voltage sources and current constraints, assigning proper metal layers for each power domain is an important issue. Figure 1 [10] is a substrate with two dies. Layers 2 and 4 are GND for noise shielding. Since the power domains of the two distinct dies are disjointed, we are able to easily assign them in layer 3. Nevertheless, taking Figure 2 [11] with multiple power domains, drawn in different colors, as an example, this may not be the case when there are multiple and complex power domains within a modern low-power chip design. Therefore, the compatibility of these power domains could impact the layer assignment result. Conventionally, the package substrate is manually designed by layout engineers. However, manual design is time-consuming and error-prone. Since the power pins of the same power domain must be connected together, we are capable of analyzing power-pin locations for power domain compatibility

evaluations. In this work, we are motivated to develop a power domain layer assignment algorithm to reduce the power domain design time as well as to maintain power delivery quality.

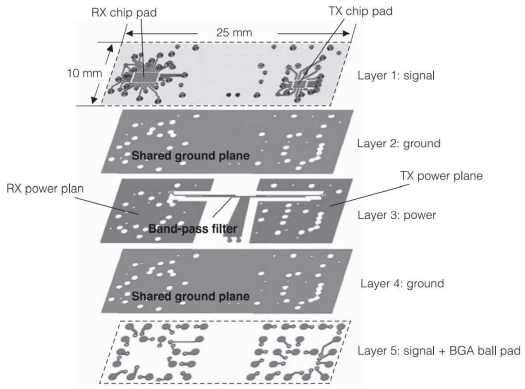


Fig. 1. Substrate layer design.

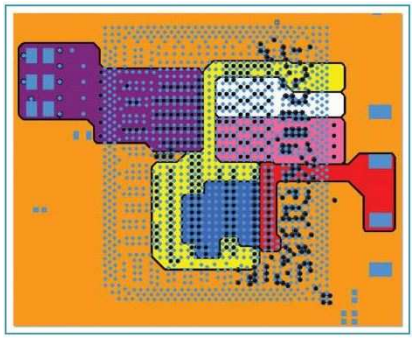


Fig. 2. Power Plane Cuts.

B. *Problem Definition*

In package substrate design, a power domain can be divided into various shapes, such as monotone polygon, orthogonal polygon, convex polygon, concave polygon or polygon with hole. In order to maintain power integrity, we use convex polygons to estimate the shape of a power domain. Based on the estimated power domain convex polygons, our basic idea is to scatter power domains with large convex area to different metal layers and to assign area-compatible power domains to the same metal layer. Table I lists the notations and definitions of our algorithm.

III. Layer Assignment Algorithm

Based on the obtained convex polygons, the layer assignment algorithm is divided into two stage the first stage is seed selection and the second stage is minimum-cost matching. Initially, the first step is to select a seed power

TABLE I
Notations and definitions

A(A)	The area of domain A
DomainNum	The number of domains
LayerNum	The number of layers
SubArea	Substrate area
P(A)	The number of points in domain A
C(A)	The current of domain A
CMedian	The median of current in all domains
LayerArray	The domain which stored in the each layer. Size is equal to LayerNum.
P_{AB}	Number of points which belong to A and in the B's convex hull polygon
L(A)	Domain A which in the layer
E(A)	Expand convex polygon A
DL	A sorted domain list in descending order
PE_{AB}	Number of points which belong to A and in the E(B) but without in B
SeedCost(A,B)	$A(A \cap B) + \frac{P_{AB}+P_{BA}}{P(A)+P(B)} * SubArea$
AssignCost(A,B)	$P_{AB} + P_{BA} + PE_{AB} + PE_{BA}$

domain for each layer. Since the power domain with high current constraint either has a lot of pins or a large convex polygon area, our cost function prioritizes both conditions. In order to assign high current power domains to different metal layers, a power domain with current constraint greater than overall median current is selected as the seed. The algorithm can see in the algorithm 1.

Once the seed of each metal layer is selected, the second minimum-cost matching algorithm is performed to assign area-compatible power domains to proper metal layers. In the matching stage, we focus on the power domain pin issue for the remaining un-assigned power domains. Since all pins of a power domain must be connected within the polygon shape, we have to take pin positions and distributions into account. To achieve better power domain polygon shape partition, we expect to match a power domain with fewer pins overlapped by the other power domains within the same metal layer. The less intersection is the better. In addition, we need to consider the following two special cases.

1. Collinear, refer to Figure 3, the domain points are (almost) in the same line. We believe the collinear power domains can be easily partitioned since the edge of the substrate can be used for cutting. Therefore, we slightly extend the convex polygon of the power domain to find out the collinear pins.

2. Completely overlapped power domain, like a polygon with hole. The smaller power domain polygon can be perfectly placed in the larger power domain polygon. We believe the two power domains can be easily partitioned. Therefore, we set the cost to zero.

The algorithm can see in the algorithm 2.

Algorithm 1: Seed selection

input :
Calculate *SeedCost* pairs of two power domains A and B. Sort the *SeedCost* pairs as a list *SCList* in descending order.
The SCList.A and SCList.B stands for power domains A and B.
output: Each Layer of their first domain
Step1:
foreach *SCList* **do**
  if $A(SCList.A \cap SCList.B) > 0$ **then**
    if $C(SCList.A) > CMedian$ **then**
      $Seed \leftarrow A$
    end
    if $C(SCLis.B) > CMedian$ **then**
      $Seed \leftarrow B$
    end
  end
end
Step2:
if *Seed is not enough* **then**
  foreach DL **do**
    if $C(DL_A) > CMedian$ && $DL_A \neq seed$ **then**
      $Seed \leftarrow DL_A$
    end
  end
end

Algorithm 2: Minimum-cost Matching

input : Domain list & each layer array
output: Assign all power domain
foreach DL_A **do**
  foreach $B \leftarrow LayerArray$ **do**
    calculate $AssignCost(A, B)$
    if $perfectly\ overlap$ **then**
      $Cost = 0$
    end
  end
  put the smallest cost in the layer
end

IV. Experimental Results

We develop our framework using C++ programming language on a Linux Ubuntu18.04 workstation with 1.80 GHz Intel i7-8550U CPU and 16 GB memory. We use an industrial flip-chip design in our preliminary experiment. Assume that the number of power domain metal layers is 4. Figures 4(a) - 4(d) are selected seed domains for individual metal layers. Both the convex polygon size and the power pin number of selected domains are large among all power domains. Nevertheless, from Figures 4(b) - 4(d), there are still quite a few unoccupied local sub-regions in PDN5, PDN6, and PDN7. Since some unassigned small power domains may be compatible to the seed power domain, the seed power domain and unassigned power domains could be assigned to the same metal layer.

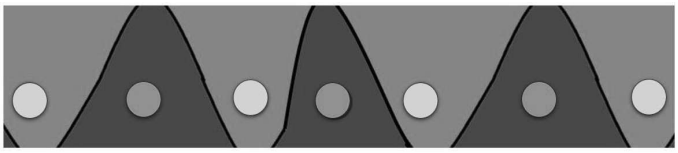
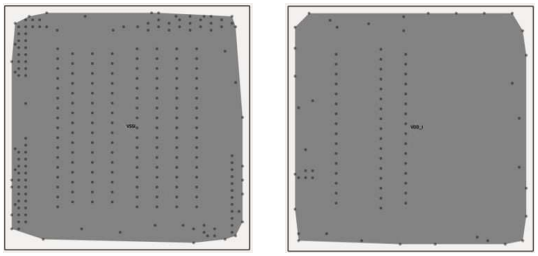
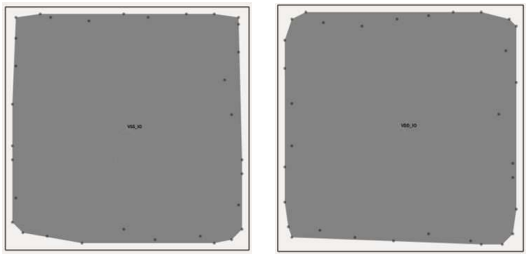


Fig. 3. Collinear point cutting.



(a) Convex polygon of PDN3. (b) Convex polygon of PDN5.

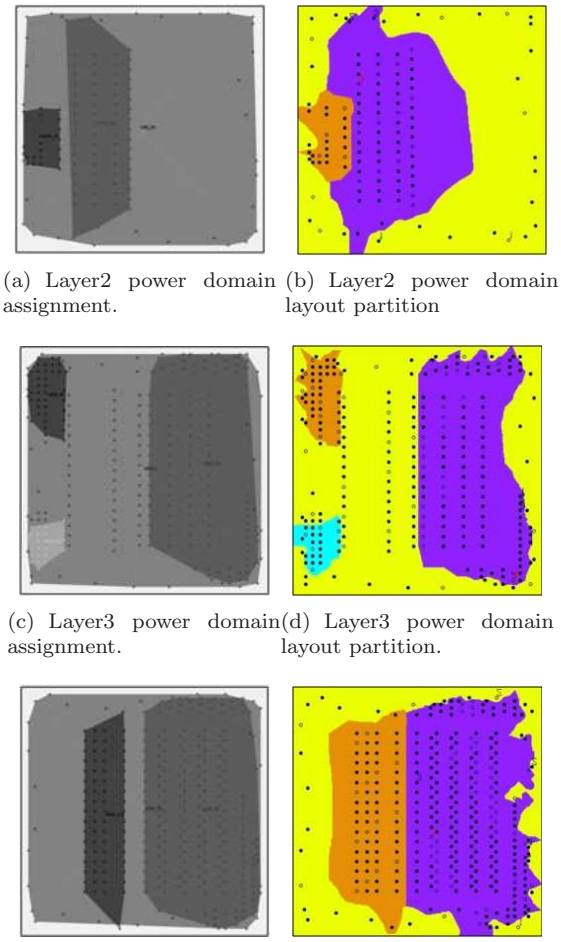


(c) Convex polygon of PDN6. (d) Convex polygon of PDN7.

Fig. 4. Convex polygons of selected seed power domains.

After the seed selection, we assign all power domains by applying our minimum-cost matching algorithm. Finally, power domain sets PDN3, PDN2, PDN5, PDN10, PDN1, PDN6, PDN8, PDN9, and PDN4, PDN7, PDN11 are assigned to four individuals layers, respectively. Once when the layer assignment is complete, a heuristic geometrical partition engine is used to generate layout partitions [12]. Figure 5 depicts the final layer assignments and layout partitions of layer2 to layer4. Since there is only one power domain (PDN3) in layer1, the assignment result and layout partition are omitted. From Figure 5, the assigned power domains can be easily partitioned into simple polygon shapes within each individual layer. Therefore, our seed selection and minimum-cost matching algorithms achieve good assignment results. With the help of

our layer assignment algorithm, package substrate power domain layout design automation could be realized.



(a) Layer2 power domain assignment. (b) Layer2 power domain layout partition

(c) Layer3 power domain assignment. (d) Layer3 power domain layout partition.

(e) Layer4 power domain assignment. (f) Layer4 power domain layout partition.

Fig. 5. Power domain assignment and layout partition.

V. Conclusion

In this work, we propose a two-phase automatic power domain layer assignment methodology for package substrate design. In seed selection phase, critical power domains with larger area conflict with other domains are assigned to separate metal layers. In minimum-cost matching phase, unassigned power domains are assigned to proper metal layers taking power pin distribution into account. Experimental results demonstrate the effectiveness of our layer assignment algorithm for the follow-up polygon layout partition. With our proposed methodology, power domain layer assignment could be performed in early design stage. Combined with a geometrical layout partition engine, the partitioned polygon shapes provide an efficient initial for layout engineers to start with.

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