On Optimization of Power Network Synthesis for Multiple Power Domain Designs

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***Abstract*—In this paper, we propose a methodology that synthesize and optimize the power network for design with multiple power domains. An architecture is presented to represent the power network with presence of sleep transistors. The power network is numerically modeled to RC network using Modified Nodal Analysis and solved using Conjugate Gradient Method.**

Regarding to IR drop effect mitigation, an optimization technique is proposed based on Simulated Annealing that minimize total power stripe area while satisfying a given IR drop constraint. In consideration of multiple power domains, the given power domains are represented in tree-like structure and our algorithm is recursively applied to synthesize and optimize the power network for each power domain in a hierarchical fashion.

The proposed methodology is integrated to commercial design tool and experimented on real design case for evaluation. To ensure practical aspect of our approach, evaluation is performed on latest digital design commercial tool. Design data and parameters are extracted using Open Access. The result of our algorithm is fed back to latest commercial tool for final IR and EM analysis. Our algorithm is tested on both industrial testcase and academic MCNC benchmark. Comparing to conventional P/G network, using our power network synthesis can achieve 31% - 35% reduction in total P/G area while satisfying maximum 10% IR-drop constraint.

I. Introduction

Power network synthesis today faces several challenges due to technology advancement. Generally, conventional power network includes one set of P/G network and power ring surrounding the chip. However, to achieve more cost effective fabrication and better performance, multiple macro blocks are generally integrated in one die to reduce fabrication cost and increase performance due to reduction in interconnect delay.

More macro blocks in one die imply more power consumption per unit area. To optimize power consumption for power demanding design, the concept of **Multiple Supply Voltage** (MSV) is proposed. The basic idea of MSV is to let critical modules operate at higher driving voltage while less critical modules operate at lower voltage. Integrating multiple macro blocks in one die also introduces the concept of **Multiple Power Domain** (MPD). Since not every macro block operates at same driving voltage, each macro block has its own unique power network and driving voltage to efficiently control power consumption [5].

A. Previous Works on Power Network Optimization

Power network synthesis and optimization have always been a highly regarded research topic in both academia and industry. Numerous techniques and algorithms are proposed to facilitate the process.

In [4] and [3], power network is synthesized on three dimensional circuit. Falkenstern *et al.* modify B*-Tree representation to accommodate 3D-floorplan design and use Simulated Annealing to perturb a given design. Chen in attempt to prevent IR drop violation. [3] implement their algorithm using [4] as base engine and propose a new architecture that insert TSV in 1:2:4 ratio which can achieve smaller number of TSV insertion compared to [4]. In both [4][3], optimization primarily focuses on perturbation of floorplan and pays little attention on power network.

In [7], both sleep transistor and power network are simultaneously considered during power network synthesis. A fake via concept is used to model sleep transistor's channel resistance. Optimization of power network is based on heuristic rules that size up or down if design rule is violated. In attempt to prevent IR-drop violation, Zhou *et al.* [9] presented a floorplanner using small grid to estimate the maximum IR drop of the floorplanning. However, it lacks consideration on pitch of power stripe.

B. Our Contributions

With new emerging low power techniques and design methodology, today's IC design flow has unprecedented number of restriction and constraints. Relieving these constraints may produce experimental result with significant improvement, however, it may also pose difficulty in practical use.

In this paper, we propose a methodology that hierarchically construct power network for multiple power domain design with pre-placed sleep transistors and level shifters. Our algorithm is integrated to industry design flow at post-placement stage and experimented on real design. Final result is a completed design that is LVS/DRC clean and evaluated using commercial IR/EM verifier.

In consideration of IR-drop effect, we model the given power network using Modified Nodal Analysis(MNA)[6] and solves the linear system using Conjugate Gradient Method to enhance runtime. We propose an optimization methodology based on Simulated Annealing to determine appropriate number of stripes and decide appropriate position to place the power stripe with minimal width that satisfies the given IR constraint.

The organization of the remaining paper is as follows. First, the structure of power network in multiple power domains is presented. RC network is then constructed and converted to MNA matrix. The MNA matrix is solved using Conjugate Gradient Method to obtain voltage value at each node. To minimize power stripe area without violating given IR-drop constraint, we propose an optimization technique based on Simulated Annealing to modify the structure of power network. Finally, a hierarchical architecture is presented in application to multiple voltage design.

II. Structure Representation

Since accurate dynamic current is not available at power planning stage, the power analysis conducted in this paper assumes worst case average current using a universal activity factor on all cells. Fig. 1 is an illustration of the RC network in a macro block. For multiple power domains, the power network in a macro block consists of core's power supply and macro block's its own power supply. The top two layers are the core's VDD power supply, the middle two layers are macro block's power supply and the bottom two layers are connected to ground.

Fig. 2 is an illustration of a design's power network with multiple power domains. The given design is partitioned into several bins. In a single power domain design, each bin has one horizontal and one vertical power network passing through. For each overlapping region of horizontal and vertical power stripe, it corresponds to two nodes in RC network. Fig. 3 is an overhead view and three dimensional view of the overlapping region.

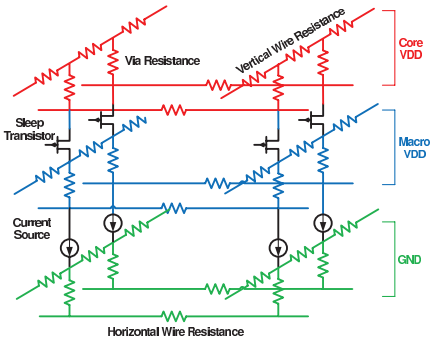


Fig. 1. An illustration of RC network for a macro block's power domain.

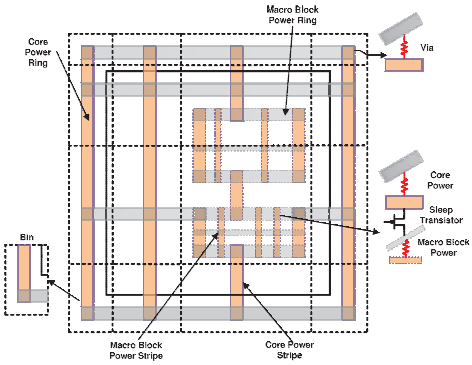


Fig. 2. An illustration of power network in a multiple power domain design. The two small rectangles are two macro blocks with its power network. The RC network in core's power domain has 4 layers. The RC network in macro block's power domain has 6 layers due to presence of sleep transistors.

For each node, there is wire resistance in left(front) and right(back) direction depending on the direction of power stripe. Wire resistance is calculated using Eq. (1) in which ρ denotes sheet resistance. In Eq. (2), via resistance is calculated by dividing resistance of one single via by the total number of vias in the overlapping area of two stripes. The width of wire stripe is adjusted such that they are integer multiple of via's width and length. In Eq. (3), the current value for given a bin_i is the summation of all current by all cells in bin_i. Resistance of sleep transistor, R_{sleep} is calculated by dividing total sleep transistor resistance by all n nodes which is described in Eq. (4).

$$R_{wire} = \rho \cdot \frac{l_{wire}}{w_{wire}} \tag{1}$$

$$R_{via} = \frac{R_{via}}{\#ofvias} = \frac{R_{via}}{\frac{l_{wire}}{l_{via}} \cdot \frac{w_{wire}}{w_{via}}} \tag{2}$$

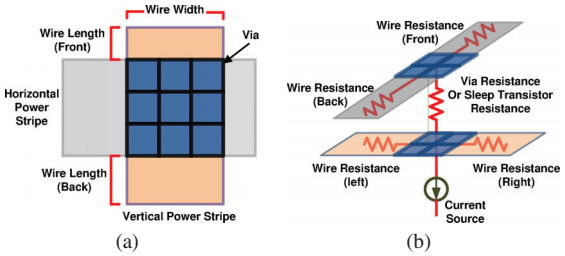
$$I_i = \sum_{j \in i}^{n} \frac{P_{cell_j}}{V_{drive}} \tag{3}$$

$$R_{sleep} = \frac{m \cdot R_{sleep}}{n} \tag{4}$$

The RC Network can be constructed using MNA as shown in Eq. (5) in which G is the conductance matrix, x is the unknown voltage value for all nodes and b is the given current value for all nodes.

$$Gx = b \tag{5}$$

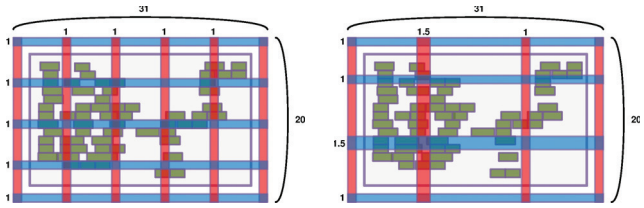
Since G is a sparse positive definite matrix, it can be solved efficiently using conjugate gradient method.



(a) (b)

Fig. 3. An illustration of intersection area between a horizontal and vertical stripe. (a) is an illustration of intersection area which can insert 9 vias. (b) is an illustration of three dimensional view for (a). The resistance between a horizontal and vertical stripe is either via's resistance or sleep transistor's resistance. The current source is the sum of all current drawn from all cells in a particular bin.

III. Power Network Optimization



(a) Area = 275.0 $unit^2$ (b) Area = 229.5 $unit^2$

Fig. 4. Placement of power stripe (a). Uniform placement of power stripes (b) Non-uniform placement of power stripes.

It is crucial to place power stripe in region where it is most effective to reduce IR-drop effect. Although Fig. 4(b) has less power stripe area compared to Fig. 4(a), the IR-drop between the two may not be so different since Fig. 4(b) has wider power stripe placed in region where cells are more congested.

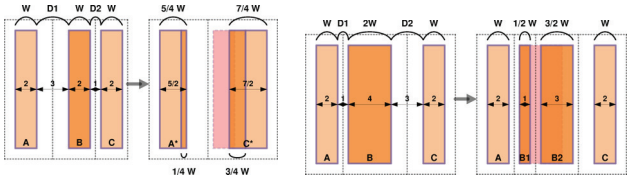
In this paper, the goal of power network optimization is to minimize total power network area including power stripe and power ring while maintaining IR-drop value above a certain threshold. The detail mathematical description is described in Eq. (6). Given an IR-drop value constraint, minimize total number of power stripes and minimize width of power stripe. The width of each power stripe must be bounded within the maximum and minimum width constraint.

$$\begin{aligned} \text{minimize} \quad & \sum_{i}^{n} l_i \cdot w_i \\ \text{subject to} \quad & IR_n < IR_{target} \\ & |j_m| < j_{EM} \\ & w_{min} \leq w_i \leq w_{max} \end{aligned} \tag{6}$$

- l_i is the length of power stripe i
- w_i is the width of power stripe i
- w_{min}, w_{max} are the minimum and maximum wire width constraint
- IR_n is the IR drop value on node n
- IR_{target} is given IR drop constraint
- j_m is the current density of VDD network branch m
- j_{EM} is the given maximum current density constraint

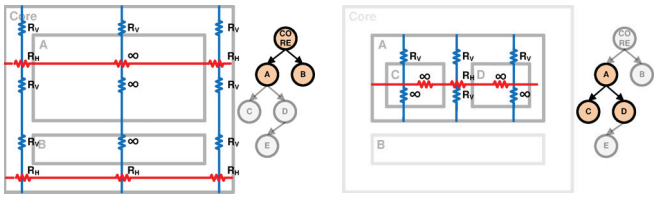
During optimization stage, an initial power network is generated with uniform spacing and width. Simulated Annealing is then applied to randomly select a power stripe and randomly scale stripe width up or down. The increase or decrease of wire width is scaled by unit of via width(height) for maximum utilization of via.

To ensure that the given IR-drop constraint is not violated, voltage value for each node is examined after each iteration of Simulated Annealing, if IR-drop constraint is violated,



(a) (b)

Fig. 5. An illustration to remove or insert a stripe. (a) removes stripe in center and distribute stripe width to two adjacent stripes. (b) split stripe in center to two stripes and determine wire width based on distance to two adjacent stripes.



(a) (b)

Fig. 6. An illustration of power network synthesis during recursive flow. (a) synthesize power network for core's power domain. (b) synthesize power network for power domain A.

the generated solution is discarded. Eq. (7) describes the cost function used during Simulated Annealing. x_n denotes solution generated at iteration n. $P(x_n)$ is the probability to accept solution x_n. A_n is the total power stripe area at iteration n. If total power stripe area at iteration n is less than power stripe area in last iteration, the solution is undoubtedly accepted. Otherwise, solution is accepted with a probability that decreases exponentially as iteration number n increases.

$$p(x_n) = \begin{cases} 0 & \text{if } IR_n - IR_{min} \geq 0, \\ 1 & \text{if } A_n < A_{n-1}, \\ 1 - e^{\frac{\triangle A}{T}} & \text{if } A_n \geq A_{n-1} \end{cases} \tag{7}$$

Since wire width is bounded by maximum and minimum width constraint, the method for power network reduction in [8] is applied to split a stripe when its width exceeds maximum constraint and remove a stripe when its width is less than minimum constraint. The method proposed in [8] is to accelerate simulation of a given power network. Power grid is reduced to a coarser form by removing certain stripes from power network and distributes the width of removed stripes to adjacent stripes.

$$\begin{aligned} \Delta W_A &= W_{A^*} - W_A = W_B \cdot \frac{D_2}{D_1 + D_2} \\ \Delta W_C &= W_{C^*} - W_C = W_B \cdot \frac{D_1}{D_1 + D_2} \end{aligned} \tag{8}$$

We apply the same concept to remove a certain stripe when it violates minimum width constraint. The width of removed stripe is added on to two adjacent stripes. The incremented width on two adjacent stripes is proportional to its distance to the removed stripe. Fig. 5(a) is an illustration of when a certain stripe is removed. Stripe B is removed from power network, the area of stripe B is distributed to two adjacent stripes, A and C. Since stripe C is closer to stripe B, it gains larger portion of added stripe area. The increment on stripe width is described in Eq. (8) where width of stripe A and C are increased from W_A and W_C to W_{A*} and W_{C*} respectively.

Similar concept is extended to split a certain stripe when it violates maximum width constraint. Fig. 5(b) is an illustration of when a certain stripe is split to two stripes. Stripe B is split to stripe $B1$ and $B2$. Similar to reduction of stripe width, the width of $B1$ and $B2$ is determined based on distance to adjacent stripes. However, stripe with larger distance away from adjacent stripe will have larger portion of width. Splitting in wire width is described in Eq. (9). Since stripe $B2$ is farther away from stripe C compare to stripe $B1$ and A, $B2$ has larger share in stripe width.

$$\begin{aligned} W_{B1} &= W_B \cdot \frac{D_1}{D_1 + D_2} \\ W_{B2} &= W_B \cdot \frac{D_2}{D_1 + D_2} \end{aligned} \tag{9}$$

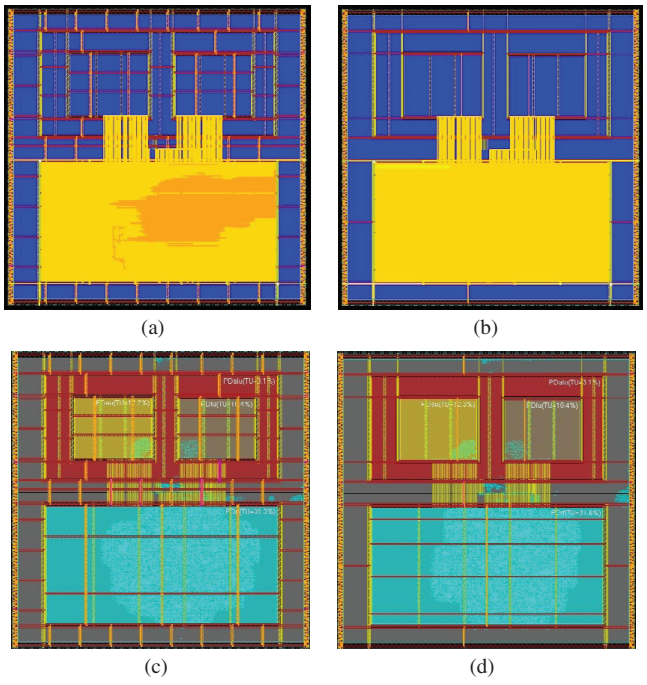
IV. Application to Multiple Power Domains

Given a power domain P, the synthesizer will first check whether if there exist any child power domain in P. The power ring will be first synthesized for every child power domain $C \in P$. After power ring for every child domain C is synthesized, the RC network using structure described in Section II will be constructed for domain P.

When synthesizing power network in domain P, cell's power consumption for every child domain is disregarded. Thus, to obtain an equivalent open circuit, resistance value within the boundary in any child domain C is set to infinity. In Fig. 6(a), power network is synthesized in core's power domain, resistance value for node positioned within power domain A and B is set to infinity.

After the power network for a given power domain finishes synthesis, it will begin to synthesize power network for every child domains. The process is conducted in recursive top-down hierarchical fashion and terminates until power network is synthesized for every power domain.

V. Experimental Result



(a) (b) (c) (d)

Fig. 7. Power analysis using EDI 10.1 for RF Domain and power network of the entire chip. (a) is the power analysis using uniform power stripe. (b) is the power analysis using our power network synthesis. (c) is the power network using uniform power stripe. (d) is the power network using our power network synthesis.

Experiment on power network synthesis is conducted on latest commercial platform, Encounter Digital Implementa-

TABLE I
COMPARISON ON MAX. IR DROP VALUE, AVG. IR DROP VALUE AND TOTAL P/G AREA BETWEEN USING UNIFORM P/G NETWORK AND OUR POWER NETWORK SYNTHESIS ON REAL DESIGN IN TSMC 90NM TECHNOLOGY USING COMMERCIAL TOOL FOR POWER ANALYSIS

Domain	Max. IR Drop (unit: Voltage)			Avg. IR Drop (unit: Voltage)			Total P/G Area (unit: um^2)		
	Uniform (**A**)	Our(**B**)	(**B-A**)	Uniform (**C**)	Our(**D**)	(**D-C**)	Uniform	Our	Imprv. (%)
Core	0.8985000	0.8960860	0.0002360	0.8988370	0.8995800	0.0007430	153563.50	105350.70	31.40%
RF	0.8462080	0.8504790	0.0042710	0.8520050	0.8551610	0.0031560	84390.54	75929.33	10.03%
ALU	0.8991570	0.8992920	0.0001350	0.8995460	0.8995480	0.0000020	79874.71	54755.01	31.45%
AUI	0.8990200	0.8980770	-0.0009430	0.8994400	0.8985500	-0.0008900	34030.02	12247.06	64.01%
LUI	0.8991520	0.8980890	-0.0010630	0.8994740	0.8985790	-0.0008950	73452.58	11701.66	84.07%
VSS	0.0207923	0.0264744	-0.0056821	0.0091606	0.0110730	-0.0019125	213401.90	155311.90	27.22%
Total	0.8462080	0.8504790	**0.0042710**	0.8520050	0.8551610	**0.0031560**	638713.25	415295.70	**34.98%**

TABLE II
COMPARISON ON DISTRIBUTION OF NODES BASED ON THEIR IR-DROP VALUE BETWEEN UNIFORM P/G NETWORK AND OUR POWER NETWORK SYNTHESIS

Range		Core		RF		ALU		AUI		LUI		VSS	
Voltage	IR-Drop	Uniform	Our	Uniform	Our	Uniform	Our	Uniform	Our	Uniform	Our	Uniform	Our
0.860-0.900	4.40%	221889	144648	4019	16727	246012	218354	100291	80922	99592	80577	478186	342866
0.853-0.860	5.18%	0	0	71343	255136	0	0	0	0	0	0	0	0
0.847-0.853	5.93%	0	0	297155	68946	0	0	0	0	0	0	0	0
0.840-0.847	6.70%	0	0	193	0	0	0	0	0	0	0	0	0

TABLE III
COMPARISON ON MAX. IR DROP VALUE, AVG. IR DROP VALUE AND TOTAL P/G AREA BETWEEN USING UNIFORM P/G NETWORK AND OUR POWER NETWORK SYNTHESIS ON MCNC BENCHMARK USING OUR POWER ANALYSIS

Testcase			Max. IR Drop (unit: Voltage)			Avg. IR Drop (unit: Voltage)			Total P/G Area (unit: um^2)		
Name	Dim.	Domain #	Uniform (**A**)	Our(**B**)	(**B-A**)	Uniform (**C**)	Our(**D**)	(**D-C**)	Uniform	Our	Imprv. (%)
ami33	903*1400	3	0.946383	0.937916	-0.008467	0.960249	0.953919	-0.006330	220000	181600	17.45%
ami49	7084*5300	3	0.949905	0.934546	-0.015359	0.968006	0.957972	-0.010034	320000	220200	31.19%
apte	6858*6805	3	0.946770	0.927354	-0.019416	0.975778	0.967034	-0.008744	320000	194700	39.16%
xerox	5124*3913	3	0.944210	0.926310	-0.017900	0.974807	0.964426	-0.010381	260000	173400	33.13%
Avg.					**-0.015285**			**-0.008872**			**31.26%**

tion (EDI) 10.1[1] to evaluate performance of our algorithm. TSMC 90nm technology file is used during the experiment and activity factor is set to 0.2 for all cells.

Table I presents the result on IR-drop value and total power network area using uniform power stripe and our power network synthesis. Uniform power stripe in this context refers to power stripes that are equally spaced apart and uniform in stripe width. Regarding to Table I, using our power network synthesis can achieve roughly 35% reduction in total power network area while maintaining equivalent IR-drop value in all domains. Fig. 7 is the power analysis and power network using both approaches. It can be observed that the region with high IR-drop value in Fig. 7(a) is removed in Fig. 7(b).

Table II presents the distribution of IR-drop value in intervals. Since domain **core, alu, aui, lui and VSS** have very low utilization rate, it is unaffected to IR-drop effect regardless of which kind power network synthesis is used. Comparing our algorithm with uniform power stripe, 75% of node falls in 5.18% IR-drop interval using our power network synthesis and 80% of node falls in 5.93% IR-drop interval using uniform power stripe. The difference in node number is due to different in number of power stripes used.

In addition to TSMC 90nm design, we also experiment our power network synthesis on a set of academic benchmark [2]. In Table III, tradeoff between reduction in P/G network area and increase in IR-drop value can be observed. An average of 31.26% reduction in total P/G area with increase of 15.29% increase in maximum IR-drop value.

According to our observation, position of power stripe affects IR-drop value significantly. More power stripes does not necessarily entail better IR-drop value, power stripes also need to be carefully placed to reach maximum effect. The reason of better IR-drop distribution is because our algorithm will place power stripe in region having more power consumption and remove stripe or decrease stripe width in region with less power consumption.

VI. CONCLUSIONS

In this paper, we proposed a power network synthesis methodology for multiple power domain. Our optimization technique can avoid redundant power stripe added in region with no significant IR drop and position power stripe in region where minimizing IR-drop effect is most effective. Comparing to previous works, our work is integrated to industrial design flow which demonstrates the practical aspect of our algorithm. Result produced using our power network synthesis shows consistency on both academic and industrial benchmarks.

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