An Integrated Smart Current Sensing Current-Mode Buck Converter

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***Abstract*—This paper presents an integrated circuit implementation of a high efficiency current-mode buck converter over a wide loading current. The converter adaptively operates as Pulse-Width Modulation (PWM). An on-chip current sensing technique is employed to reduce external components and no extra I/O pins are needed for the current-mode controller. A soft-start operation is designed to eliminate the excess large current during the startup of the regulator. The DC-DC converter was fabricated in 0.35 μm CMOS process with 2P4M. The range of the supply voltage is from 2 to 5V, which is suitable for single-cell lithium-ion battery.**

***Index Terms*—current-mode controller, current-sensing circuit, DC-DC converter, pulse-width modulation(PWM), switch-mode power converter.**

I. INTRODUCTION

DC-DC switching converters are important building blocks for integrated power management ICs [1]-[4]. Many power management blocks with a battery voltage range (Li-ion: 2.7-4.2V) and have to operate at supply voltage of 5V. DC-DC switching converters are widely used due to their high efficiency and high output current which make them suitable for portable electronic devices. It is necessary to minimize the power loss in order to extend the operating time of the device. On the other hand, the trend in portable devices is to use the architectures that incorporate less number of external components and move toward to a single chip.

The current-mode control requires much simpler compensation network compared to the voltage-mode control. Moreover current-mode control is superior in dynamic response to voltage-mode control [5]-[7]. A compact high efficiency current mode integrated buck (step-down) converter is shown in Fig. 1. In this paper, a buck converter with high power-conversion efficiency that operates with 2-5V supply voltage is achieved by using the proposed pulse width modulation (PWM) control circuits.

II. PROPOSED DC-DC CONVERTER

A. Error Amplifier for Compensation

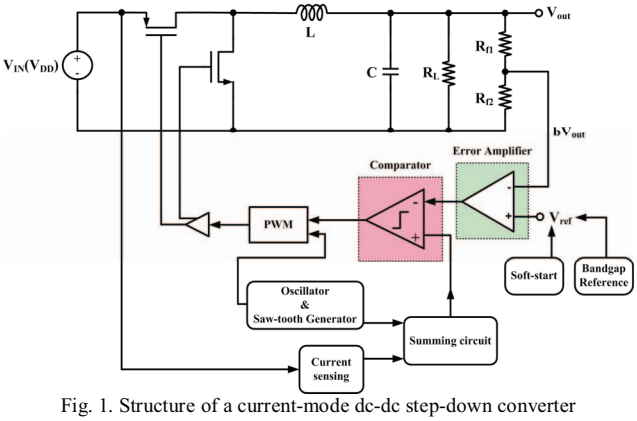


Fig. 1. Structure of a current-mode dc-dc step-down converter

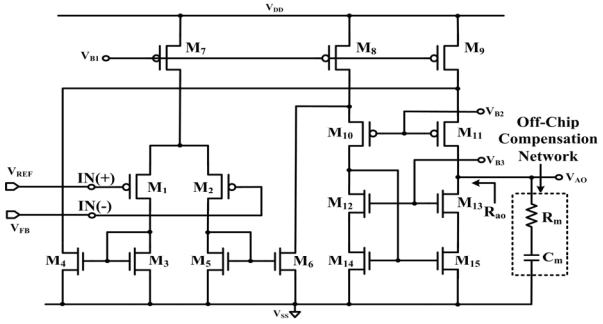


Fig. 2. Schematic of the error amplifier

The error amplifier detects and amplifies the difference between the feedback voltage and the bandgap reference voltage. A comparator generates PWM signal according to the output signal of the error amplifier. The switch control logic circuit turns on and off the power transistor in accordance with the PWM signal. This paper implements a slew rate of an error amplifier of 100 V/μs, which can improve large signal transient response. The error amplifier and compensation network are also called as a compensator, as shown in Fig. 2. The transfer function of the compensator is given by

$$T(s)=\frac{V_{AO}}{V_{FB}}=-G_m R_{ao}\frac{1+sC_m R_m}{1+sC_m\left(R_{ao}+R_m\right)} \qquad (1)$$

where R_{ao} is the output resistance and G_m is the transconductance of the error amplifier. A zero and a pole are represented in the following:

$$f_{zero} = \frac{1}{2\pi\left(C_m R_m\right)} \tag{2}$$

$$f_{pole} = \frac{1}{2\pi C_m\left(R_{ao} + R_m\right)} \tag{3}$$

B. Bandgap Reference

The complete schematic of the designed bandgap voltage reference is presented in Fig. 3. The sum of a signal I_{PTAT} (Proportional To Absolute Temperature current) and a signal I_{CTAT} (Complementary proportional To Absolute Temperature current) through a resistor generates a reference voltage. The reference voltage can be adjusted by coefficients (α、β) and the resistor (R_{REF}). Therefore, the reference voltage value can be properly adjusted to a desired value, which is independent of supply voltage and temperature. Simulation performance is capable of realizing a temperature coefficient of 7ppm/℃ shown in Fig. 4. The output of the reference voltage is

$$V_{REF} = \left(\alpha \times I_{PTAT} + \beta \times I_{CTAT}\right) R_{REF} \tag{4}$$

C. Soft-Start Circuit

The soft-start circuit is shown in Fig. 5(a). The soft-start method charges a capacitor with a constant current generating a ramp voltage V_{start}. This ramp voltage is used as reference voltage during startup ($t < t_{soft\text{-}start}$). When the ramp voltage is greater than V_{REF}, the reference voltage V_{ref} is fixed to V_{REF} (Fig. 5(b)). The soft-start time $t_{soft\text{-}start}$ can be calculated as:

$$t_{soft-start} = V_{REF} \times C_{soft} / I_B \tag{5}$$

V_{REF} is the reference voltage which determines the end of startup. C_{soft} is the capacitor and I_B is the charging current. In order to obtain longer soft-start time, we need low charging current and high capacitance capacitor.

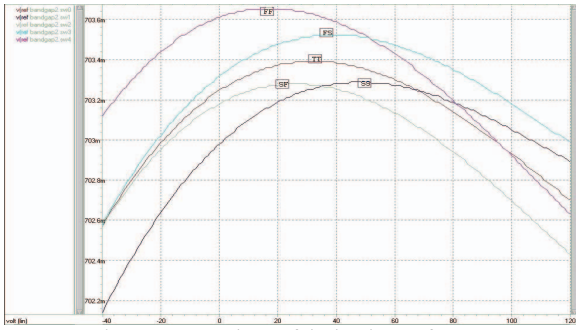
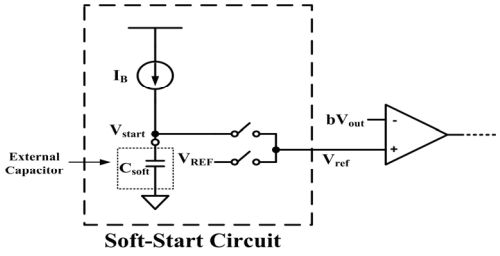
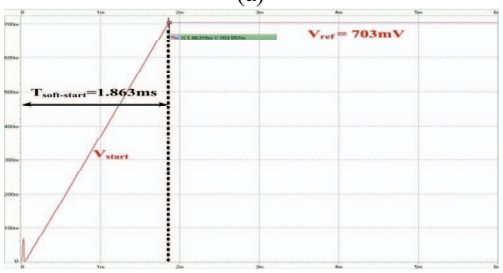


Fig. 4. Output voltage of the bandgap reference



(a)



(b)

Fig. 5. (a) Schematic of the soft-start circuit. (b) Operation of soft-start Circuit

D. Oscillator

The oscillator circuit consists of one comparator and one capacitor as shown in Fig. 6. The ramp voltage V_{ramp} is limited within V_H and V_L (Fig. 7). The oscillator frequency is determined by V_H, V_L, C_{S1} and I_{C1} as the following equation:

$$f_{osc} = \frac{I_{C1}}{C_{S1} \cdot \left(V_H - V_L\right)} \tag{6}$$

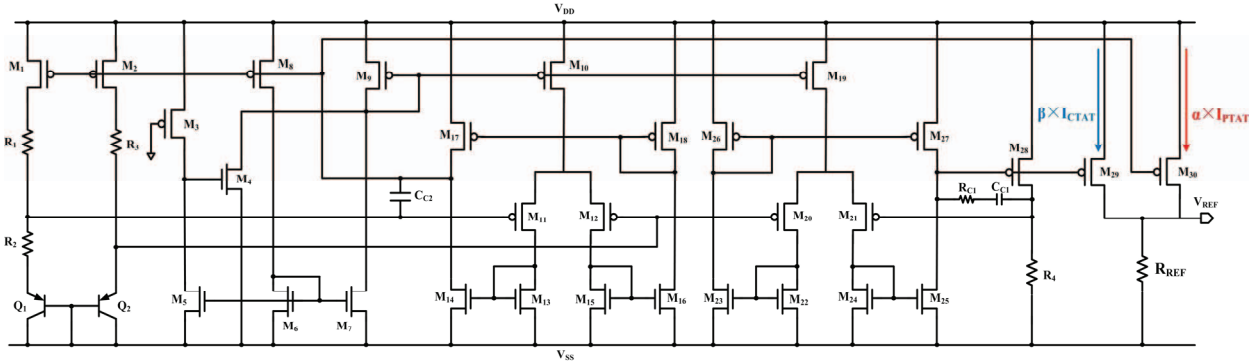


Fig. 3. Complete schematic of the bandgap reference

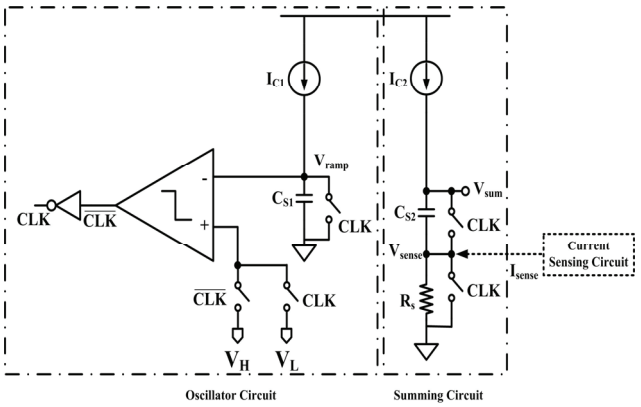


Fig. 6. Schematics of the oscillator and the summing circuit

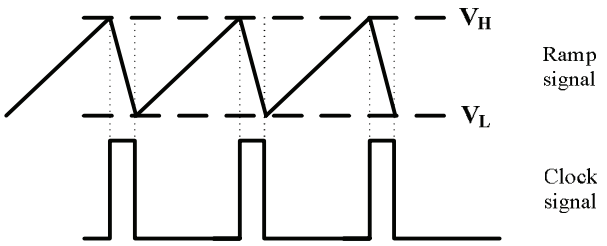


Fig. 7. Operation of the oscillator

E. Summing Circuit

The summing circuit contains one capacitor and one resistor to sum the slope compensation ramp and inductor sensing current, as shown in Fig. 6. The summing circuit does not use a V-I converter, and it is a simpler and smaller area circuit. The charge current I_{C2} is equal to oscillator charge current I_{C1}, and C_{S1} is equal to C_{S2}. The I_{sense} comes from Inductor current sensing circuit and is injected into Rs to generate a sensing voltage V_{sense}. The capacitor's bottom voltage rises from ground to V_{sense}, and the capacitor's top voltage rises from V_{ramp} to $V_{ramp}+V_{sense}$. Therefore, The V_{sum} is equal to V_{ramp} and V_{sense}.

F. Inductor Current Sensing Circuit

The inductor current sensing circuit is realized by a matched PMOS transistor M1 with respect to 1/N of the aspect ratio of Power PMOS transistor M_P, as show in Fig. 8. During the converter ON state, M_P and M_{S2} turn on. Due to virtual short by amplifier, node A and node B voltage are equal. The inductor current, I_L, flows through the power PMOS transistor, mirroring current to transistor M_1. I_{M1}, the sensing current, equals I_L scaled by a factor, 1/N, 1/1000 or 1/2000 for example. As a result, the current I_{M1} on the sensing side is much smaller than the current I_L, which saves power consumption. The current I_{sense}, which passes through the on-chip resistor in the summing circuit, is different from I_{M1} because some current flows through the amplifier as bias current. This bias current $2I_B$ is much smaller than I_{M1} and it does not affect the sensing current accuracy.

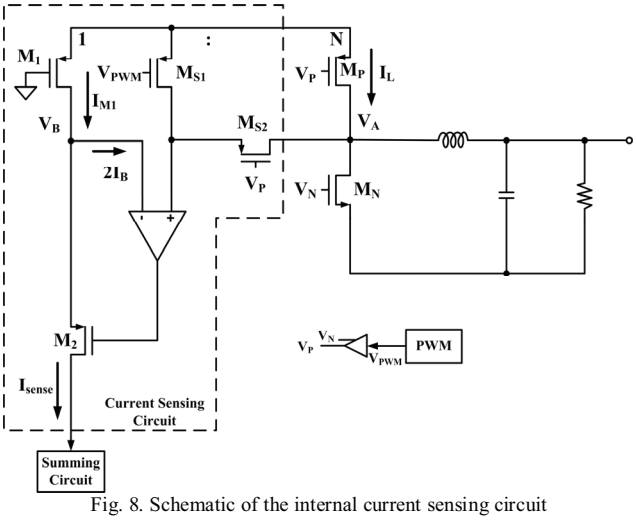


Fig. 8. Schematic of the internal current sensing circuit

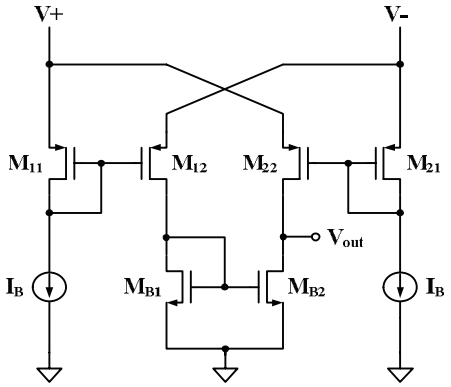


Fig. 9. Schematic of the sensing amplifier

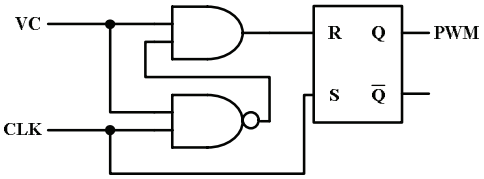


Fig. 10. Schematic of the pulse-width generator

The amplifier used in the proposed sensing circuit is constructed by two constant current sources I_B, two current mirrors with matched PMOS transistors in cross-coupled connection, and one current mirror with matched NMOS transistors (Fig. 9).

G. Pulse-Width Modulation Generator

In general, a SR latch is used for the pulse-width modulation generator. However, when S=R=1, this combination is called a restricted combination as both outputs are zeros, it breaks the logical equation $Q = \sim \overline{Q}$. In order to avoid this situation, adding AND and NAND logic gates ensures that both inputs of SR latches are not high simultaneously (Fig. 10).

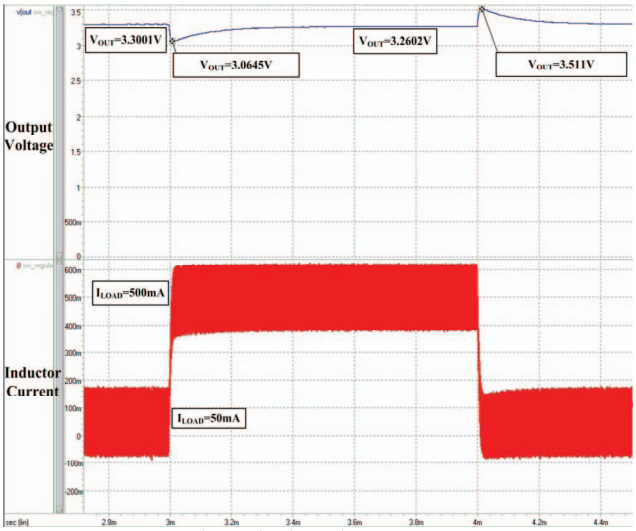


Fig. 11. load transient response

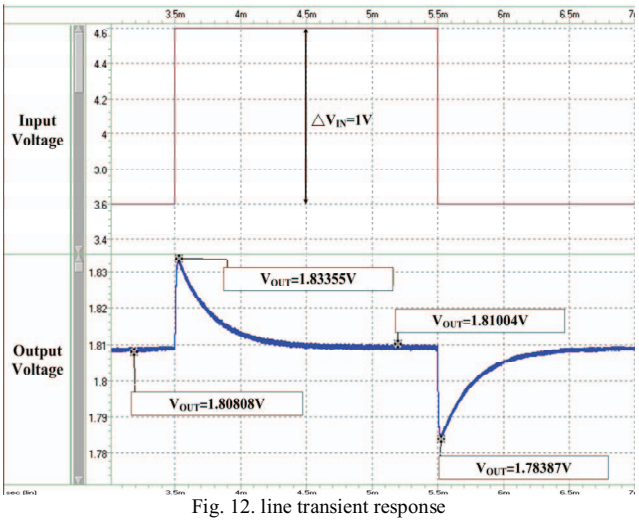


Fig. 12. line transient response

III. RESULTS

The output voltage of the converter with the load current is varied from 50 mA to 500 mA, is shown in Fig. 11. The load regulation is 39.9 mV/mA. The line regulation is 1.96 mV/V. The output voltage of the regulator at the line transient response, as the supply voltage is varied from 3.6 V to 4.6 V, is shown in Fig. 12. The efficiency can reach 95.6% with load current of 50mA and 96.8% with load current of 500mA. This DC-DC converter achieves the maximum output current of 1A. A summary of the proposed DC-DC converter performance is shown in Table I.

IV. CONCLUSION

In this paper, an integrated current-mode buck converter with smart current sensor has been introduced, analyzed, and implemented. As a result, the buck converter can achieve high power efficiency over a wide loading current.

TABLE I. SUMMARY OF THE DC-DC CONVERTER PERFORMANCE

Technology	TSMC 2P4M 0.35μm CMOS process
Inductor L (off-chip)	10μH
Capacitor C (off-chip)	10μF
Switching Frequency	1MHz
Efficiency	95.6% @ 50mA; 96.8% @ 500mA (V_{IN}=5V,V_{OUT}=3.3V)
Input Voltage Range	2.0 to 5.0V
Load Regulation	0.089 mV/mA
Line Regulation	1.96 mV/V
Max. Output Current	1000mA

In load transient response and line transient response, the converter can accurately recover to target voltage. In addition, the converter can operate with supply voltage from 2 to 5V, which is suitable for portable devices with a single-cell lithium-ion battery. An on-chip current sensing technique is employed to reduce external components and no extra I/O pins are needed for the current-mode dc-dc step-down converter.

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