Linear Time Estimation of Full-Chip Statistical Leakage Current

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Abstract - In this paper, we propose a method for estimating the leakage current of a circuit under process parameter variations. The proposed method needs only O(N) computation time where N is the number of gates in circuit, and is faster than Monte Carlo and Wilkinson's method. Experimental results show that the proposed method is effective in estimating statistical full-chip leakage current. Errors for 99 percentile value of full-chip leakage current are within 1%.

I. Introduction

Leakage power is increasing drastically with technology scaling. It is approximately 50% of the total active power in the 90nm technology node [1,2] and has gone up by 4× in the 45nm node [3]. It is important to accurately estimate leakage currents so that they can be accounted for during design, and so that it is possible to effectively optimize the total power consumption of a chip.

Leakage currents can arise due to varying phenomena. Reference [4] lists eight different mechanism of leakage current. Not all these components of leakage are important during normal modes of operation, and subthreshold leakage (Isub) and gate leakage (Igate) currents are the most significant components of leakage current.

The subthreshold leakage current, Isub, is exponentially dependent on the threshold voltage, Vth, and Vth is observed to be most sensitive to gate oxide thickness, Tox, and effective gate length, L, due to short-channel effects [5]. The subthreshold leakage current is estimated by the following empirical curve-fitted model [6].

$$Isub = a_0 \exp(a_1+a_2L+a_3L^2+a_4Tox^{-1}+a_5Tox) \quad (1)$$

The gate leakage current is also estimated by the following empirical curve-fitted model [6].

$$Igate = b_0 \exp(b_1+b_2L+b_3L^2+b_4Tox+b_5Tox^2) \quad (2)$$

With the advent of deep sub-micron technologies, the variations of process parameters L and Tox are increasing. Under process parameter variations, Isub and Igate can no longer be considered to be constants, but must be modeled as random variables. Using first-order Taylor expansion at the nominal values of process parameters to exponents of leakage current models, (1) and (2), we have following leakage current variation models.

$$Isub = \exp(A_0 + A_1dL + A_2dTox) \quad (3)$$

$$Igate = \exp(B_0 + B_1dL + B_2dTox) \quad (4)$$

where, A_0 and B_0 are nominal values of exponents, dL and dTox are variations of L and Tox respectively, which are random variables. We assume these random variables are normal.

On the other hand, in modeling the process parameter variations like dL and dTox, it is important to model die-to-die (D2D) parameter variations and within-die (WID) parameter variations separately [7]. D2D parameter variations result from lot-to-lot, wafer-to-wafer, and global variations within wafer, and give the same parameter variations to each gate on a chip. WID parameter variations result from random noises during fabrication, and can be divided into correlated or systematic parts and independent parts. In general, a process parameter variation dp (ex. dL, dTox) can be modeled as

$$dp = dp_{D2D} + dp_{WID} , \quad (5)$$

where dp_{D2D} is D2D variation and dp_{WID} is WID variation. dp_{D2D} and dp_{WID} are normal random variables and are independent.

Using these process variation models, leakage current I (Isub or Igate) can be modeled as follows.

$$I = \exp(Y_0 + Y_{WID} + Y_{D2D}), \quad (6)$$

where Y_0 is a nominal value of the exponent and Y_{WID} is WID variation of the exponent and Y_{D2D} is D2D variation of the exponent. Y_{WID} consists of WID variation of L and Tox. Y_{D2D} consists of D2D variation of L and Tox. Y_{WID} and Y_{D2D} are normal. Thus, the distribution of leakage current is lognormal.

The full-chip leakage current can be now computed by summing up leakage current of each gate in the circuit

$$I_{full\text{-}chip} = \Sigma_{i=1,..,N} \quad Isub_i + Igate_i , \quad (7)$$

where N is the total number of gates in the circuit. As each leakage component is modeled as a lognormal distribution (6), the full-chip leakage distribution can simply be found by summing up the distribution of the lognormals:

$$I_{full\text{-}chip} = \Sigma_{j=1,..,M} \exp(Y_{0,j} + Y_{WID,j} + Y_{D2D,j}), \quad (8)$$

where M is total number of lognormals to sum. Since D2D components must be correlated each other, the computation of full-chip leakage current involves finding a sum of correlated lognormals.

Monte Carlo simulations provide a method to compute sum of correlated lognormals. But they are very expensive in terms of time complexity.

Theoretically, the sum of lognormal distributions is not known to have a closed form. However, it may be well approximated again as a lognormal using Wilkinson's method [6,8,9]. But complexity for Wilkinson's method is $O(N^2)$ where N is the total number of gates in the circuit. It is far from practical for actual large circuits.

In this paper, we propose a method for estimating full-chip statistical leakage current in O(N) computation time. We applied the proposed method to actual chip designs. Using the proposed method, we can estimate 99 percentile value of full-chip statistical leakage current within 1% error compared to Monte Carlo simulations. The proposed method may be suitable to estimating statistical full-chip leakage current at LSI design stage.

The rest of the paper is organized as follows. In Section II, we review the statistical leakage current model using in this paper. In Section III, the full-chip statistical leakage current computing methods are proposed. Section IV shows the experimental results. Section V concludes this paper.

II. Statistical Leakage Current Model

In this section, we will describe statistical leakage current models using in this paper.

In the previous section, leakage current I (Isub or Igate) can be modeled by (6).

According to delay variation model of [7], we assume WID variations are independent for each gate and D2D variations are modeled by one random variable for a chip. We model leakage current I (Isub or Igate) as follows.

$$I = \exp(a + b\alpha + c\beta), \qquad (9)$$

where α is WID variation parameter which is independent on each gate and β is D2D variation parameter which is the same for all gates. α and β are standard normal random variables whose means are 0 and variations are 1.

The total leakage current, Ioff, of a gate can be modeled as

$$\begin{aligned} Ioff &= Isub + Igate \\ &= \exp(a_{sub} + b_{sub}\alpha + c_{sub}\beta) \\ &\quad + \exp(a_{gate} + b_{gate}\alpha + c_{gate}\beta). \qquad (10) \end{aligned}$$

According to the Wilkinson approximation, we model Ioff by another lognormal random variable as follows.

$$Ioff = \exp(A + B\alpha + C\beta), \qquad (11)$$

the coefficients A, B, and C can be estimated by empirical curve-fitting.

We use this leakage current (Ioff) model in this paper.

III. Proposed Method

In this section, we will present the method for estimating full-chip statistical leakage current. It consists of the following two steps.

Step 1: Calculation of approximate distribution of full-chip leakage current distribution.
Step 2: Calculation of percentile leakage current value from the approximate distribution.

This method needs only O(N) computation time. Thus we can say that the proposed method is practical for actual large circuits. We describe Step1 at Section 3.1 and Step2 at Section 3.2.

3.1 *Approximate Distribution of Full-Chip Leakage Current Distribution*

Using total leakage current model (11) of a gate in the previous section, the full-chip leakage current $I_{full\text{-}chip}$ can be expressed as follows:

$$I_{full\text{-}chip} = \Sigma_{i=1,..,N} \exp(A_i + B_i\alpha_i + C_i\beta), \qquad (12)$$

where N is the total number of gates in the circuit. α_i (i=1,..,N) is WID variation parameter which is independent for each gate and β is D2D variation parameter which is the same for all gates. α_i and β are standard normal random variables.

We approximate $I_{full\text{-}chip}$ to another lognormal random variable

$$I_{full\text{-}chip} \sim \exp(P + Q\beta), \qquad (13)$$

by the following ideas:

- WID parameter α_i is independent for each gate. According to law of large numbers [10], WID parameters are replaced by their mean value,
- Inspired by Wilkinson's method, we approximate sum of lognormals to another lognormal.

WID components $\exp(B_i\alpha_i)$ (i=1,..,N) of full-chip leakage current (12) are independent each other. Otherwise D2D components $\exp(C_i\beta)$ (i=1,..,N) are strongly correlated. Therefore D2D components are dominant.

According to law of large numbers [10], variations of WID components are canceled and WID components can be replaced by their mean values if N is sufficiently large. The mean of WID component $E[\exp(B_i\alpha_i)]$ can be computed as follows (see [6,8,9]):

$$E[\exp(B_i\alpha_i)] = \exp(B_i^2/2) \qquad (14)$$

Therefore, the full-chip leakage current $I_{full\text{-}chip}$ can be approximated as follows:

$$I_{full\text{-}chip} \sim \Sigma_{i=1,..,N} \exp(A_i + B_i^2/2 + C_i\beta) \qquad (15)$$

Next, inspired by Wilkinson's method, we approximate sum of lognormals in (15) to another lognormals as follows:

$$\Sigma_{i=1,..,N} \exp(A_i + B_i^2/2 + C_i\beta) \sim \exp(P + Q\beta) \qquad (16)$$

Our approximation strategies are as follows:

- Both sides of (16) are equal when β is zero. This means that typical values of both sides of (16) are equal.

● Means of both sides of (16) are equal.

Using these strategies, we can compute P and Q which are coefficients of the right side of (16) (see Appendix) and the full-chip leakage current $I_{full\text{-}chip}$ can be approximated as follows:

$$I_{full\text{-}chip} \sim \exp(P + Q\beta), \quad (17)$$
$$P = \log[\Sigma_{i=1,..,N} \exp(A_i+B_i^2/2)], \quad (18)$$
$$Q^2 = 2\log[\Sigma_{i=1,..,N} \exp(A_i+B_i^2/2+C_i^2/2)] - 2P, \quad (19)$$

where we assume that Q is non-negative.

Differ from the Wilkinson's method which requires $O(N^2)$ computation time, the proposed method needs only O(N) computation time where N is total numbers of gates in circuit.

3.2 *Computation of Statistical Full-Chip Leakage Current*

Using the approximated full-chip leakage current proposed in the previous subsection, we can estimate percentile leakage current of a circuit.

The full-chip leakage current $I_{full\text{-}chip}$ can be approximated by lognormal random variable as follows:

$$I_{full\text{-}chip} \sim \exp(P + Q\beta), \quad (20)$$

where P and Q are coefficients as (18) and (19). β is standard normal D2D variation parameter on a circuit.

x percentile leakage current l_x is defined as the probability that the full-chip leakage current is less than l_x is x%. Using the approximated leakage, l_x can be estimated as follows:

$$\begin{aligned} x\% &= \text{Probability}\{ I_{full\text{-}chip} < l_x \} \\ &\sim \text{Probability}\{ \exp(P + Q\beta) < l_x \} \\ &= \text{Probability}\{ \beta < (\log(l_x)-P)/Q \} \quad (21) \end{aligned}$$

Since β is standard normal, we can compute l_x using the table of the normal distribution [10]. For example, 99 percentile leakage current l_{99} can be estimated as follows :

$$(\log(l_{99})-P)/Q = 2.33$$
$$l_{99} = \exp(P + 2.33Q) \quad (22)$$

This means that the probability that a standard normal random variable is less than 2.33 is about 99%.

Similarly, 10 and 50 percentile leakage current l_{10}, l_{50} also can be estimated as follows:

$$l_{10} = \exp(P - 1.29Q) \quad (23)$$
$$l_{50} = \exp(P) \quad (24)$$

Figure 1 shows our algorithm of estimating 99 percentile full-chip leakage current. Our algorithm needs only O(N) execution time where N is total numbers of gates in circuit.

Algorithm: 99 percentile full-chip leakage current estimation
Input: $(A_1,B_1,C_1),\ldots,(A_N,B_N,C_N)$: leak model coefficients of each gate
Output: l_{99} : 99 percentile full-chip leakage current

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1. x=0
2. y=0
3. For i=1,…,N
4.   x = x + exp(Ai+Bi^2/2)
5.   y = y + exp(Ai+Bi^2/2+Ci^2/2)
6. P = log(x)
7. Q^2 = 2log(y) – 2P (Q>0)
8. l99 = exp( P + 2.33Q )
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Figure 1. 99 percentile full-chip leak estimation

IV. Experimental Results

We applied the proposed full-chip statistical leakage current estimation to four chip data, DataA, DataB, DataC, and DataD.

These data consist of 100,000 gates which are selected from actual chip designs.

We estimate 10, 50, and 99 percentile full-chip leakage current of these four data. For comparison purposes, we performed Monte Carlo simulations with 10,000 runs on these data. Figure 2 shows a naive algorithm of computing 99 percentile value of full-chip leakage current.

Tables 1 to 4 show percentile full-chip leakage current comparison of the proposed method and Monte Carlo. Leakage current values in tables are scaled. Using the proposed method, full-chip statistical leakage current can be estimated within 2% error compared to Monte Carlo analysis. Especially, 99 percentile value of full-chip leakage current can be estimated within 1% error.

Dominant run time of the proposed method is the number of gates sum of exponents (Step 3 to 5 in Figure 1). That is almost equal to twice as one sample generation time (Step 3 to 6 in Figure 2) in Monte Carlo. Therefore the proposed method is the half of iteration time (5,000 in this case) faster than Monte Carlo.

Table 1. Scaled percentile leakage current of DataA

percentile	Proposed	MC	error
10%	5.1082	5.1246	0.322%
50%	6.0867	6.0848	0.032%
99%	10.4739	10.5323	0.555%

Table 2 Scaled percentile leakage current of DataB

percentile	Proposed	MC	error
10%	4.3157	4.3296	0.321%
50%	5.2271	5.2243	0.054%
99%	9.3105	9.3678	0.612%

Table 3. Scaled percentile leakage current of DataC

percentile	Proposed	MC	error
10%	1.1045	1.1215	1.511%
50%	2.0581	2.0569	0.056%
99%	6.3336	6.3972	0.993%

Table 4. Scaled percentile leakage current of DataD

percentile	Proposed	MC	error
10%	1.2686	1.2865	1.387%
50%	2.3626	2.3621	0.022%
99%	7.2636	7.3305	0.912%

Algorithm: 99 percentile full-chip leakage current computation
Input: $(A_1,B_1,C_1),\ldots,(A_N,B_N,C_N)$: leak model coefficients of each gate
Output: I_{99} : 99 percentile full-chip leakage current
1. For i=1,..,10000 2. β_i = standard normal random number 3. $x_i = 0$ 4. For j=1,…,N 5. α_j = standard normal random number 6. $x_i = x_i + \exp(A_j+B_j\alpha_j+C_j\beta_i)$ 7. $\{y_1,\ldots,y_{10000}\} = \mathrm{sort}\{x_1,\ldots,x_{10000}\}$ $(y_1<\ldots<y_{10000})$ 8. $I_{99} = y_{9900}$

Figure 2. 99 percentile full-chip leak computation by Monte Carlo

V. Summary and Conclusions

In this paper, we proposed an estimation method of full-chip statistical leakage current which needs only O(N) computation time where N is the number of gates in circuit. The proposed method is faster than Monte Carlo and Wilkinson's method.

We applied the proposed method on four actual chip data. Using the proposed method, we can estimate 99 percentile of full-chip leakage current within 1% error much more efficiently compared with Monte Carlo.

Therefore the proposed method may be suitable to estimating statistical full-chip leakage current at LSI design stage.

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Appendix Approximation of Sum of Lognormals

We explain the method proposed in Section 3.1, which approximate sum of lognormals,

$$\Sigma_{i=1,\ldots,N} \exp(A_i + B_i^2/2 + C_i\beta) \qquad (A1)$$

to a lognormal,

$$\exp(P+Q\beta). \qquad (A2)$$

Where A_i,B_i,C_i (i=1,..,N) are known coefficients and β is a standard normal random variable. We calculate unknown coefficients P and Q.

Approximation strategies are as follows:

- (A1) and (A2) are equal when β is zero.
- Means of (A1) and (A2) are equal.

From the first strategy, we give the following equation.

$$\Sigma_{i=1,\ldots,N} \exp(A_i + B_i^2/2) = \exp(P) \qquad (A3)$$

Means of lognormal random variables can be computed easily as in [6,8,9]. From the second strategy, we give the following equation.

$$\Sigma_{i=1,\ldots,N} \exp(A_i+B_i^2/2+C_i^2/2) = \exp(P+Q^2/2) \qquad (A4)$$

From (A3) and (A4), we can calculate coefficients P and Q as follows.

$$P = \log[\Sigma_{i=1,\ldots,N} \exp(A_i + B_i^2/2)] \qquad (A5)$$

$$Q^2 = 2\log[\Sigma_{i=1,\ldots,N} \exp(A_i + B_i^2/2 + C_i^2/2)] - 2P \qquad (A6)$$