Panel Discussion

Challenges for Future System Design and Verification

Panelists:

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Abstract

Process shrinking does not stop, and tons of transistors can be integrated in one chip. We also have 3D-IC for integrating a memory chip on a CPU chip or so, and novel non-volatile memory technologies seem to be available in the near future. We can use such huge and various resources to implement highly parallel information systems. However the design, synthesis, and verification become complicated because of the system complexity, the unreliable behavior of devices such as the process variation, single event upset, etc.

Power issue is also very important in system design. After 311 earthquake and the related nuclear plant problem in Japan, energy supply has been paid attention from the point of view of the sustainable life, and power consumption of information systems are discussed seriously since information systems become the basis of social activities and such systems cannot be stopped.

Based on those observations, we would like to discuss about the problems and solutions on future system design and verification in the panel. 5 panelists gathered from various areas will clarify images of promising future systems, problems and prospective solutions on electronic design automation of parallel systems, reliability issues, power harvesting issues, memory issues, and massively parallel system issues, etc.