A Two-Step BIST Scheme for Operational Amplifier

Jun Yuan

Electronic and Photonic System Engineering,
Kochi University of Technology,
Kami-City, Kochi, Japan, 782-8502
Tel : 0887-57-2212
Fax : 0887-57-2120
e-mail : 138007b@gs.kochi-tech.ac.jp

Masayoshi Tachibana

Electronic and Photonic System Engineering,
Kochi University of Technology,
Kami-City, Kochi, Japan, 782-8502
Tel : 0887-57-2212
Fax : 0887-57-2120
e-mail : tachibana.masayoshi@kochi-tech.ac.jp

Abstract - This paper presents a two-step Built-in Self-Test (BIST) scheme and its implementation for Operational Amplifier (Opamp). In addition to the catastrophic faults, the proposed technique can particularly detect the capacitance variation in the compensation capacitor by combining the current-based test with the offset-based test to detect the physical defects in the Opamp. The circuit-level simulation results of the proposed BIST system are presented to demonstrate the feasibility of the proposed BIST scheme with high fault coverage of 98%.

I. Introduction

The rapid development of Integrated Circuits (IC) fabrication technology and the advance of System-on-a-Chip (SoC) design technology have made it possible to integrate millions of transistors on a single chip including digital and analog components. These mixed-signal solutions are widely used in various applications like mobile and multimedia devices. However, due to the high integrity and complexity, production testing has become a major challenge for analog and mixed-signal circuits, especially for the analog blocks.

On the one hand, the high integration density limited the accessibility and observability to the internal component since the limited I/O pins. On the other hand, compared to pure digital circuits, analog circuits have a large number of performance parameters with a fluctuation range, so precise measure is another challenge. Hence, testing analog circuits in mixed-signal circuits is still a major challenge. As an alternative solution to the traditional off-chip test, BIST techniques, implementing both stimulus generator and response analyzer entirely on-chip, are widely applied in mixed-signal system. Conventionally, performance parameters were measured on-chip to test analog blocks, but this specification-driven BIST techniques result in high-test costs due to complex testing circuits and test time. Therefore, another structural test technique, fault-based BIST was proposed to detect the possible physical defects caused through the IC production.

As most frequently encountered parts of analog and mixed-signal circuits, Opamps test have attracted widely research attention, and a variety of test solutions have been proposed. In [1] and [2] oscillation-based test techniques were proposed to convert the Opamps under test into an oscillator by external feedback network to detect the possible faults by measuring the reasonable deviation of the oscillation frequency. In [3] and [4] transient response analysis based test techniques were proposed by converting the Opamp into a voltage follower. With respect to the fault-free circuit, performance parameters like overshoot and slew rate deviation were monitored to detect the faults in the Opamp. In [5], an AC and DC compacted testing technique was presented by monitoring and analyzing fault signatures through amplitude and offset of voltage signals. However, a sinusoidal wave was employed as test stimulus, which made this technique infeasible for on-chip test since the complex sinusoidal wave generator. In I_{DDQ} testing techniques [6] the power supply current of the Opamp under test was monitored by a current sensor in order to determine the current deviation caused by the defects, but it is hard to design a current sensor without performance degradation to the original amplifier. In [7] the negative supply current was also considered as a test variable to observe the deviations. Additionally, in [8] current signals were employed as test stimuli and injected in two nodes at the output stage of the Opamp under test, but the AC analysis on-chip circuit would cause complex circuit design for BIST application.

In above mentioned test techniques for Opamps, oscillation-based test techniques are hard to implement due to the on-chip frequency response observation circuit. Moreover, the capacitor in the feedback network would cause high area overhead. The transient response analysis based test techniques are the most feasible for BIST technique, but some slight performance parameters deviations are still hard to monitor because of the feedback circuit in the transient test, which means the difference between faulty response and fault-free responses is too small to distinguish the faulty responses from the fault-free response by on-chip test circuits.

Thus, in this paper, a feasible two-step BIST scheme for Opamp is proposed. At the first offset-based test stage, a DC voltage is employed as test stimulus to input to the Opamp configured as comparator. And then at the second current-based test stage, a step current is injected to the compensation circuit to excite the faults in the compensation circuit.

II. Test Strategy and Technique

The input offset voltage of Opamps with differential inputs and single-ended output is defined as the differential input voltage for which the DC output voltage is midway between the supplies. The offset voltage of an Opamp is composed of two components: the systematic offset and the random offset. The former results from the design of the circuit and is present even when all the matched devices in the circuit are identical, the latter results from mismatches in supposedly identical pairs of devices [9]. It can be seen from Fig. 1, an offset compensation voltage V_{os} must be added to compensate the output value to the approximate midway between the supplies due to the impact of mismatches in the Opamp; otherwise the DC value of V_{out} might be driven to the positive or negative power supply. In fact, in order to meet the acceptable offset voltage in some applications and also to make the transistors operate in saturation region, the DC output V_{out} should be located between power supplies even without the external offset compensation. Therefore, an offset-based test is employed, the V_{out} is considered as test variable to monitor the mismatch changes caused by physical defects when the inputs of Opamp are connected to the same reference voltage V_{ref} at approximate midway between the supplies.

At the offset-based test stage, some faults are still hard to detect, especially in the compensation circuit. These faults can be detected by analyzing the frequency-domain parameters like open loop gain, phase margin and unity-gain bandwidth (GB), but on-chip test circuits for measuring frequency-domain parameters would be hard to design, and also lead to unacceptable area cost. Therefore, an alterative transforming test [10] was proposed to measure the overshoot in transient response to reflect phase margin deviation. However, some faults just cause a slight slew-rate and overshoot deviation in the transient response, and so some hard-detected faults of offset-based test are still hardly detected by the transient response test, since the on-chip testing circuit is hard to observe this kind of slight deviation. For the purpose of increasing the deviation caused by the faults in the compensation circuit, in this paper a current-based test stage is employed to detect the hard-detected faults of the offset-based test stage. The current is directly injected to compensation circuit, so the deviation caused by the possible faults in the compensation circuit can be utmost reflected by the output of the Opamp under test.

Fig. 2 shows the comparisons of the fault-free output response and faulty responses (fault_1 and fault_2 are short and 50% capacitance variation of the compensation capacitor, respectively) of an Opamp, which was simulated under current-based comparator, voltage follower and comparator configurations, respectively. And it can be seen that current-based comparator configuration caused greatest differences between faulty responses and fault-free response. Thus, the hard-detected faults can be easily detected by differentiating the faulty responses from the fault-free response.

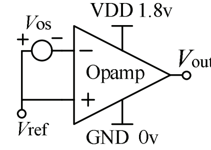

Fig. 1. The offset compensation for an Opamp.

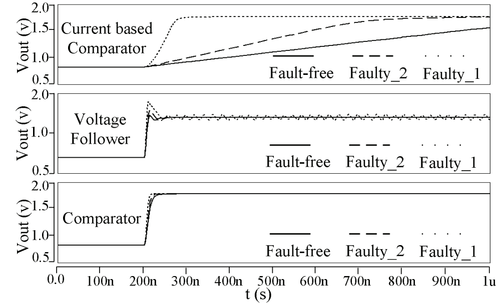

Fig. 2. The output responses of Opamp with comparator, voltage follower and current-based comparator configurations.

Consequently, in order to increase fault coverage the offset-based and current-based tests are combined to test the Opamp in this paper.

III. The Proposed Testing System and Its Implementation

A. The Proposed BIST Architecture

A basic BIST system should include three essential functions: test stimulus generation, output response analysis and test controlling. Additionally, in BIST techniques the Opamp under test should have two working modes: operation mode and test mode. Under normal working mode, the Opamp realizes the expected operation with other components by cutting the connection to the test circuits. Fig. 3 depicts the Opamp with the proposed BIST architecture, which is composed of a stimulus generator, response analyzer and isolation circuits of analog switches controlled by external controlling signals TM and TMC. The whole test procedure is controlled by these two controlling signals. In modern mixed-signal applications, these two controlling signals can be provided by the digital block on the same chip. TM is the test mode start signal; TMC was designed to connect test current to the injecting node to form a test step current.

Fig. 4 shows the faults simulation results. The marked real line represents the fault-free response of the Opamp with testing reference voltage input at offset-based test step and then a step current injected to the compensation circuit at the current-based test step. The other dotted lines show the faulty output responses with faults injection, including capacitance variation of the compensation capacitor. In offset-based test stage, the DC output voltage is monitored to determine the deviation of the DC value, and then the current-based stage is started by signal TMC to inject the step current to check the

output changing rate. Following the step current the output DC voltage rises to another stable value in a short time interval, which is called propagation delay. In real case, it is hard to precisely measure the normal output DC value due to the process variation, so ±10% fluctuation of the fault-free output is set as the acceptable band for the offset-based test. In the same way ±10% fluctuation of the rising slop is set as the acceptable band to check the deviation at the current-based test stage.

The whole test procedure is shown in Fig. 5. Initially, TM starts the test procedure by connecting the positive/negative inputs to V_t shown in Fig. 3, and output V_{out} to the response analyzer, respectively. If the DC value was in the expected range, the Opamp passed the offset-based test; otherwise the Opamp failed the whole test. And then the test current is injected to the compensation circuit, the propagation delay test circuits are activated to monitor the output changing rate based on the DC value of the offset-based test at the same time. Note that the test result of the offset-based test stage affects the current-based test by clearing or enabling the counter in order to generate a combinational test signature signal.

With the propagation delay, the output of the Opamp moves from the previous stable value to another stable value according to the change of the step current. Hence, after the test current inputs to the test node, the output of the Opamp can't immediately skip to another value owning to the effect of compensation capacitor and the parasitic capacitance of the transistors, so the propagation delay time can be employed to detect faults in the compensation capacitor and the parasitic capacitance of the transistors.

B. The Proposed BIST Implementation Circuits

Fig. 6 shows the stimuli generator including a voltage divider and a mirror current sink. The voltage divider is composed of transistors of MS0 of 2.6/0.4 μm (W/L) and MS1 of 0.6/0.4 μm (W/L). When TM starts the test, the output V_t of 0.9V is connected to the positive/negative inputs. At beginning of the current-based test, the mirror current sink, which consists of MS2 of 12/0.4 μm (W/L), MS3 of 0.54/0.4 μm (W/L) and MS4 0.54/0.4 μm (W/L), generates a 0.74μA sink current.

Fig. 7 depicts the block diagram of the designed response analyzer including three main blocks: two window comparators, a register and a 5-bit counter. The first window comparator consists of an exclusive OR gate of XOR0 and four inverters of INV01, INV02, INV11 and INV12, and the second consists of an exclusive OR gate of XOR1 and four inverters of INV11, INV12, INV21 and INV22. As it is shown in Fig. 8, the window comparators were designed to check the output value in the designed band or not and finally create a signature signal. In order to realize the band checking function, the aspect ratios of the transistors in the inverters are summarized in Table I, and other transistors used in the

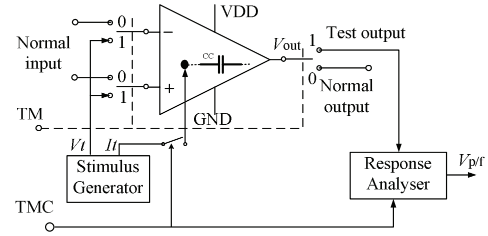

Fig. 3. The BIST architecture of the proposed test scheme.

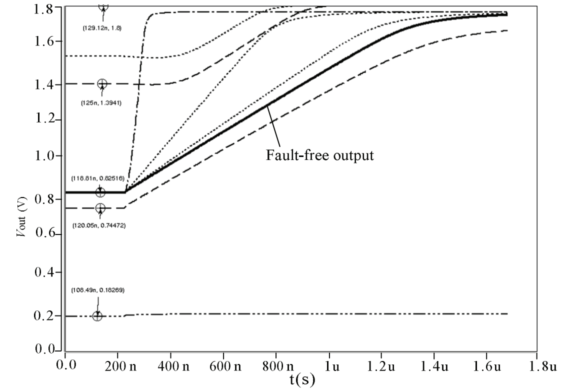

Fig. 4. Output responses of the proposed test scheme.

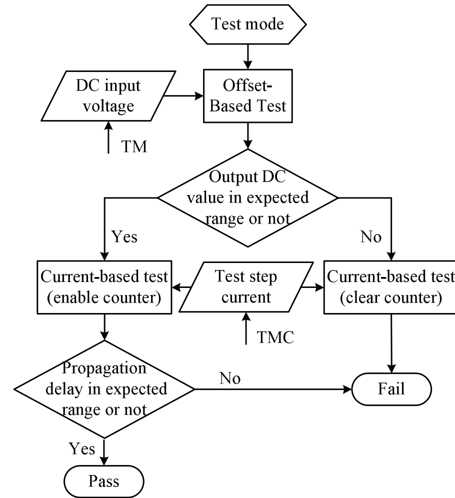

Fig. 5. The test procedure of the proposed test scheme.

TABLE I
The design of Inverters Used in Window Comparators

Elements	W/L of pMOS (μm)	W/L of nMOS (μm)
INV01, INV02	0.54/0.4	0.56/0.4
INV11, INV12	2.4/0.4	0.54/0.4
INV21, INV22	40/0.18	0.5/10

response analyzer were designed with the same aspect ratio of 0.54/0.18 μm (W/L).

The register, consisting of a set-reset latch, two OR gates, an AND gate and an inverter, was designed to store the result of the offset-based test stage and then to control the following

current-based test. In offset-based test stage, the output of SR latch indicates the result of the offset-based test. If the Opamp passed the offset-based test, SR latch outputs a digital high voltage; otherwise the current-based test stage is activated by the digital low voltage of SR latch to switch TMC to high logic, which forces SR latch to store the result of the offset-based test stage at the current-based test stage.

Additionally, the gate AND0 was designed to combine the offset-based and current-based test stage together. As it can be seen from Fig. 9, when TMC is low, the result of the offset-based test is stored in the SR latch, so AND0 outputs a digital low voltage to CLR to clear the counter because TMC forces AND0 output a low voltage. And then TMC goes high, the result of offset-based test is transmitted to CLR to control the second test stage. If the Opamp under test failed the offset-based test, the output of AND0 forces the 5-bit counter to output logic low voltage at current-based stage, thus the $V_{p/f}$ signal is derived to high. If not, the final test result depends on the propagation delay time checking of the current-based test.

The counter is a 5-bit counter, consisting of 5 T edge-triggered flip-flops with clear signal CLR. Logic low CLR forces the outputs C0-C4 to logic low, and the enable signal ENB enables the counter count edged-triggered input squared

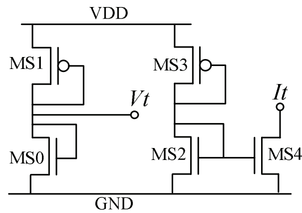

Fig. 6. The circuit configuration of the stimulus generators.

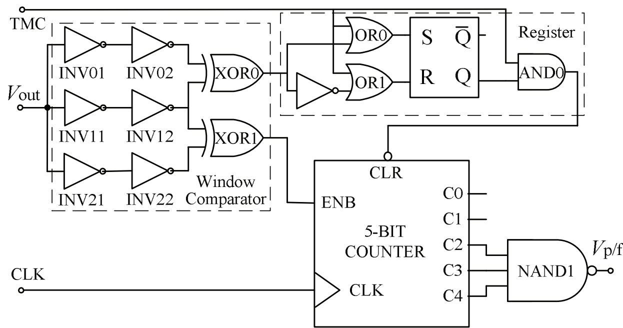

Fig. 7. Block diagram of the designed response analyzer.

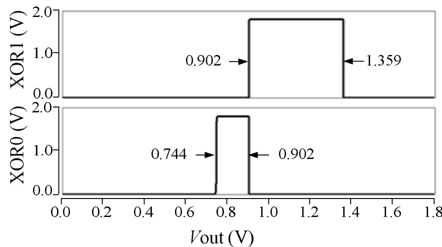

Fig. 8. The checking band of the two comparators.

clock. The 5-bit counter was designed to measure the propagation delay time by connecting the CLR and ENB to the output of the register and the second comparator.

In CMOS technology, it is hard to precisely measure propagation delay time for the fluctuating initial and final voltage value due to process variation. Thus, in this paper the time interval is chosen to differentiate the faulty output from the fault-free output. To measure the time interval, two observing values must be set in advance. The smaller observing voltage should be greater than the top value of the acceptable offset-based test band and the greater observing voltage should be smaller than the bottom value of the acceptable band of the final voltage according the current input. In our case, the two voltage observing values are setting by the boundaries of the second window comparator.

Additionally, the frequency of the input clock must be accurately selected. For a fault-free Opamp, after the two test stages the highest three output bits of the 5-bit counter, C2- C4 must be "111", so that the frequency F_{clock} can be described as:

$$(2^5\text{-}3)/T_N \leqq F_{clock} \leqq 2^5/\ T_N \tag{1}$$

where T_N is the normal time interval according to the checking voltage range for the fault-free Opamp. As it is shown in Fig. 10, T0 is the mentioned normal time interval T_N, and T1 is a faulty time interval. For the consideration of process variation,

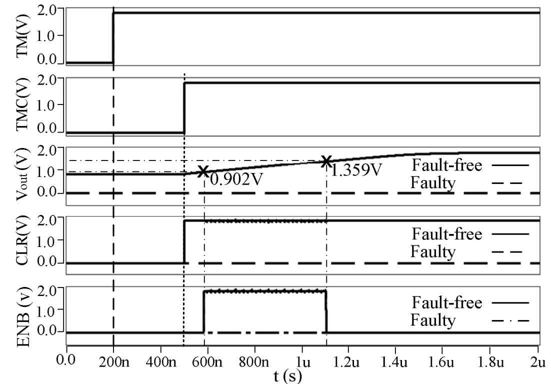

Fig. 9. Timing waveforms of the BIST system operations.

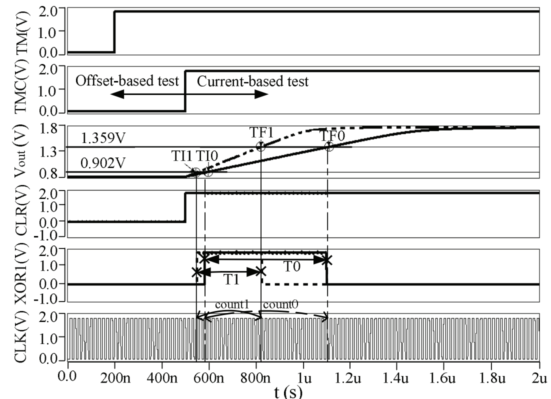

Fig. 10. The slop detection in the currrent-based test stage.

the F_{clock} can be set as 30.5/T0, in the midway between (2^5-3)/T0 and 2^5/T0.

As we have said, the test flow starts by setting TM as logic high and then the current-based test is activated by changing TMC to logic high. The two test steps are combined by the register to generate a final test signature signal $V_{p/f}$. If the Opamp passed the test, $V_{p/f}$ changes to a low digital after the activation of the current-based test, otherwise the $V_{p/f}$ remains the high digital signal. At last, the test ends by recovering TM and TMC to logic low.

IV. Simulation Results

Fault models are introduced as equivalent circuits, which are injected into DUT to reflect the behavior of realistic physical failures cased in production process. In this paper, for catastrophic 6 fault models [5] were utilized for each transistor to evaluate the proposed test system. Shorts were modeled by connecting a small resistor of 100 Ω between each pair of terminals, including Gate-Drain Short (GDS), Gate-Source Short (GSS), Drain-Source Short (DSS), Resistor Short (RS) and Capacitor Short (CS). Opens were modeled by inserting a parallel combination of a large resistor of 100 MΩ and a small capacitor of 10 fF in series into each terminal, including Drain Open (DO), Source Open (SO) and Resistor Open (RO). Particularly, Gate Open (GO) was modeled by means of grounded parallel combination of resistor and capacitor for simulating real behavior of GO.

Additionally, the parametric faults in the compensation capacitor are also considered. Because of the special physical implementation of the capacitor, which is constructed by parallel combination of smaller unit capacitors in CMOS technology, the open in the smaller unit capacitor can't be reflected by the simple open fault of capacitor like DO or GO in transistors. Thus, the possible Parallel Capacitor Opens (PCO) was modeled as capacitance variation by unit capacitance of the smaller unit capacitor.

To evaluate the proposed BIST scheme, a two-stage Opamp shown in Fig. 11, was considered as test vehicle. Through analog switches, the inputs V_{in1} and V_{in2} of the Opamp are connected to the output V_t of the stimuli generator shown in Fig. 6. The test step current is injected to the Opamp through I_t. With reference to the fault models introduced previously, a total of 50 catastrophic faults and a parametric fault for compensation capacitor existed in the two-stage Opamp.

The two-stage Opamp with on-chip BIST circuits was laid out using a 0.18-μm standard CMOS technology in Cadence environments and simulated by HSpice. For different physical design, window comparators must be carefully designed to match the acceptable band of the offset-based test, even for the same Opamp. Thus, the ratio aspects of transistors summarized in Table I must be optimized in the physical design phase. The comparison range of the window comparator would also be changed according to the process variation, so the finally the comparison range isn't exactly ±10% fluctuation of the fault-free response, but this change is slight due to the same two inverter design and is still in the acceptable range.

Due to the 5-bit counter the designed BIST circuits caused a large area cost compared to the transient response test [2], but the area overhead ratio of the BIST circuits to the original circuit would be decreased when the proposed BIST scheme is applied to a more complicated system. Table II shows the performance comparisons between the original Opamp and the Opamp with BIST circuits, which doesn't cause significant performance degradation because of the analog switches.

As it also can be known from the previous introduced test flow and BIST circuits, with the test stimuli controlled by TM and TMC, the designed BIST circuits generate a test signature signal $V_{p/f}$ to declare the Opamp under test passed or failed the test. Fig. 12 summarizes the fault simulation results that show 98% faults can be detected by the proposed BIST system. The undetected fault is the RS in compensation resistor.

The faults in transistors were mainly detected by the first offset-based test stage of the DC output checking. And the DC output voltage is much more sensitive to the faults in the transistors than the transient response test [1, 2]. For example, some faults in the current biasing circuit, which is composed of M0, M5 and M12 in Fig. 11, change the bias current and cause the open loop gain decrease of the Opamp under test. This bias current change directly excites the output stage of the Opamp and cause significant voltage deviation, but can't be reflected obviously in the transient response or is hard to capture for on-chip test circuit. So DC test can achieve high

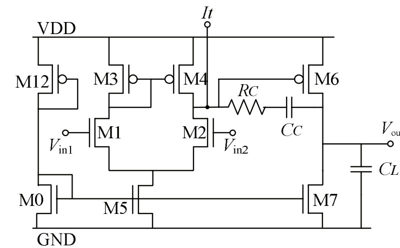

Fig. 11. The circuit configuration of the two-stage Opamp under test with inclusion of design for test.

TABLE II
Performance Comparisons between the Original Opamp and the Opamp with BIST Circuits

Performances	Simulated Values		
	Original Opamp	**Opamp with BIST circuits**	**Units**
Offset Voltage	180	180	μV
DC Gain	71.165	71.16	dB
Unity Gain Bandwidth	28.603	28.41	MHz
Phase Margin	67.366	65.898	Degree
Slew Rate	+2.83/-5.42	+2.79/-5.34	V/μS
Power Supply Rejection Ratio+/-	93.741/97.592	93.631/97.337	dB

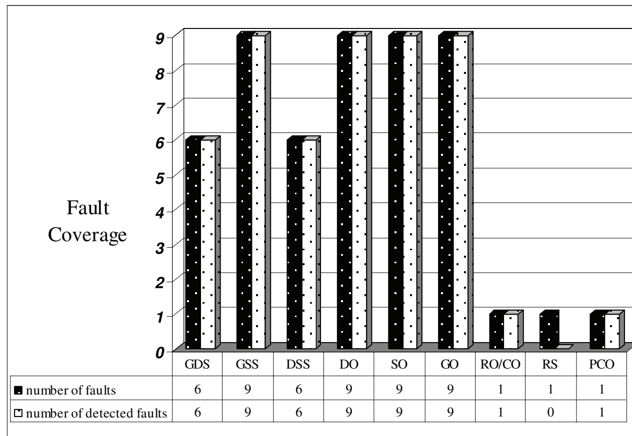

Fig. 12. Summary of the fault coverage.

fault coverage. However, this offset-based DC test is limited by the large input offset design; the DC output voltage might be derived to the power supply sides due to the large offset design. Even though this kind of large offset design is acceptable in some cases, the large offset design should be eliminated to make the transistors work in saturation region.

The current-based test was designed to assist the offset-based test in order to test the short RO/CO and capacitance variation PCO in compensation circuit.

V. Summary and Conclusions

In order to increase the fault coverage of Opamp test, this paper has proposed a BIST scheme which combines offset-based test and current-based test together to test the catastrophic faults and the parametric fault in the compensation circuit. Using 0.18-μm CMOS technology, the5-bit counter based on-chip testing circuit was implemented with a two-stage Opamp and the fault simulation has shown the proposed scheme could be an alternative and effective test approach for Opamp with high fault coverage. The proposed BIST scheme can also be applied to test other amplifiers on the same chip with different window comparators. The disadvantages of this BIST scheme is large area overhead, but this situation would be improved in the multi-amplifier complicated circuits.

Acknowledgements

This work was supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Cadence Design System, Mentor Graphics, Rohm Corporation and Toppan Printing Corporation. And it was also supported by KAKENHI (23500067) Grant-in-Aid for Scientific Research (C). The authors are grateful to Kochi University of Technology (KUT) for a Special PhD. Scholarship Program. The authors also would like to thank the numbers of our laboratory for patiently explanation about experiment device.

References

[1] J. Font-Rossello, J. Ginard, E. Isern, M. Roca and E. Garcia, “A Digital BIST for Opamps Embedded in Mixed-Signal Circuits by Analyzing the Transient Response,” *Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba,* April 2002, pp. I012-1- I012-5.

[2] I. Rayane, J. Velasco-Medina and M. Nicolaidis, “A digital BIST for operational amplifiers embedded in mixed-signal circuits,” *IEEE Symp.17th VLSI Test Symposium, San Diego. California*, April 1999, pp. 304-310.

[3] K. Arabi and B. Kaminska, “Oscillation-test strategy for analog and mixed-signal integrated circuits,” *VLSI Test Symposium, Princeton, New Jersey,* May 1999, pp. 476 – 482.

[4] K. Arabi and B. Kaminska, “Design for testability of embedded integrated operational amplifiers,” *IEEE Jouranal of Solid-State Circuits*, vol.33, pp. 573 - 581, April 1998.

[5] Wimol San-Um and M. Tachibana, “A Compact On-Chip Testing Scheme for Analog-Mixed Signal Systems Using Two-Step AC and DC Faults Signature Characterizations,” *SASIMI ‟2009, Okinawa. Japan*, pp. 428–433, March 2009.

[6] M. Roca and A. Rubio, “Selftesting CMOS operational amplifier,” E*lectronics Letters*, vol. 28, pp. 1452 - 1454, July 1992.

[7] J. Font, J. Ginard, E. Isern, M. Roca, J. Segura and E. García, “oscillation-test techniques for CMOS operational amplifiers by monitoring supply current,” *Analog Integrated Circuits and Signal Processing*, vol.33, pp. 213 – 224, November 2002.

[8] J. Velasco-Medina and M. Nicolaidis, “Current-based testing for analog and mixed-signal circuits,” *Computer Design: VLSI in Computer and Processors, Austin, Texas*, pp.576-581,October 1998.

[9] Paul R. Gray, Paul R. Hurt, Stephen H. Lewis and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed., vol. 2. Wilery: New York, 2002, pp428-pp431.

[10] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed., vol. 2. Oxford: New York, 2002, pp768-775.