A Spur-Reduction Frequency Synthesizer For Wireless Application

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Abstract—In this paper, we presents a low-spur phase locked loop (PLL) system for wireless applications. The low-spur frequency synthesizer randomizes the periodic ripples on the control voltage of the voltage-controlled oscillator (VCO) in order to reduce the reference spur at the output of the PLL. A new random clock generator is presented to perform a random selection of phase frequency detector (PFD) control for charge pump at locked state. The proposed frequency synthesizer was fabricated in TSMC 0.18-μm CMOS process. The PLL has achieved the phase noise of -93dBc/Hz at 600 KHz offset frequency and reference spurs below -72dBc.

***Index Terms*—PLL, VCO, Synthesizer**

I. Introduction

Phase noise, and Spurious-Free Dynamic Range (SFDR) are very important perspectives in designing a frequency synthesizer. For the SFDR, one of the major noise sources is the switching noise from the charge pump at reference frequency. The switching noise would modulate the control voltage and hence the output frequency of the voltage-control oscillator (VCO). Two tones will appear at the upper and lower sidebands around the carrier that reduce the SFDR performance [1]. The two tones are named reference spurs and measured using the power difference between the carrier and the spurs at a certain frequency offset (Δw) with unit of dBc, as shown in Fig. 1.

The periodic ripples on the control line of the VCO will generate reference spurs at the frequency synthesizer output. [2-4].

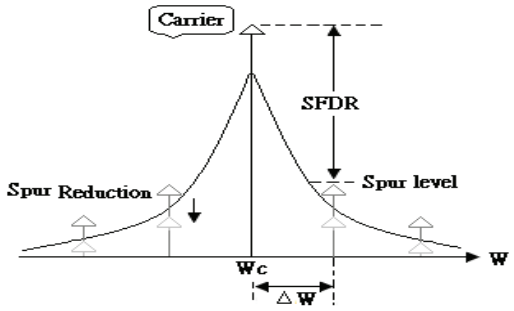

Fig.1. Frequency domain representation of spurs

$$\frac{A_{spur}}{A_{carrier}} = \frac{1}{2} \times \frac{K_{VCO} A_m}{2\pi f_{ref}} \quad (1)$$

From Eq. (1) [5], it is noted that reducing both K_{VCO} and A_m (A_m is the ripple amplitude), or increasing f_{ref} can decrease the reference spur. However, K_{VCO} is restricted to the tuning range of the specification, and f_{ref} is not a design variable in a conventional integer-N based PLL. Therefore, we can only focus on reducing the ripples on the control voltage to reduce the reference spur.

In this paper, we propose a new reference spur reduction system by randomizing and averaging ripples on the control voltage of the VCO in order to achieve a low spur level and relatively smooth spectrum. The frequency synthesizer has achieved a phase noise of -93dBc/Hz at 600 KHz offset frequency and reference spurs below -72dBc. The architecture of the proposed circuit is presented in Section II. Designs of the main building blocks are presented in Section III. The results for both synthesizer and random charge pump are given in Section IV, and conclusions are addressed in Section V.

II. Architecture

Fig. 2 shows the spur reduction Integer-N frequency synthesizer, where new techniques are proposed. The synthesizer achieves accurate setting of its output frequency by locking to a reference frequency. This locking action is accomplished through feedback by dividing down LC VCO output frequency and comparing its phase with the phase of the reference source to produce an error signal. The phase comparison operation is done through the use of PFDS which also act as a frequency discriminator when the PLL is out of lock. The low pass filter (LPF) attenuates high-frequency components of the charge pump output so that a smooth signal is sent to the LC VCO input. The LPF is typically fed by a charge pump which converts the error signal to a current waveform. A key characteristic of the Integer-N synthesizer is that a new random clock generator can randomize the output of two MUXs and hence the speeds of the charge or discharge operation of the charge

pump so that the control voltage line can randomly skip or reduce ripples. Therefore, if we could reduce the ripples generated by charge pump switches, we could expect relatively smooth voltage at the loop filter output and thus reduce spur tones in the frequency domain. This concept leads to the idea of random sampling of the charge pump output in frequency synthesizers. The proposed idea will be able to easily apply to other advanced processes.

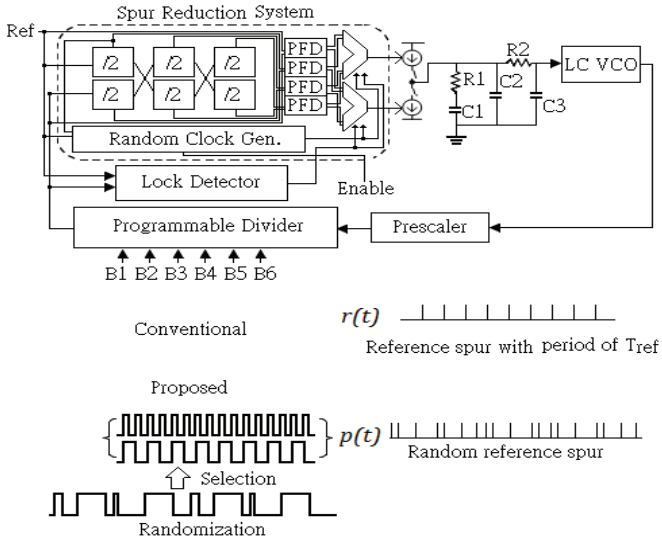

Fig.2. Architecture of the low spur frequency synthesizer

III. MAIN BUILDING BLOCKS

A. Spur reduction system

For a conventional synthesizer, while in lock, the PFD generates fast spikes that will modulate the VCO control line and generate spurious signals at the reference frequency offset, whose harmonics will reduce SFDR performance in the communication system. The spur at reference frequency is hard to filter out. Higher harmonics are usually filtered out by using the loop filter. In this paper, as shown in Fig. 3, a lock detector (LD) and a new random clock generator are used to achieve the randomization and average of the charge pump output ripple. The random clock generator provides a random signal which enables the deployment of four frequencies of charge pump operation in the synthesizer, that we call a randomized charge pump. This system to provide the four random frequencies of charge pump operation was implemented by four PFDs, six divided-by-two dividers, and two MUXs. Two MUXs will afford 00, 01, 10, and 11, which can randomize UP and DN to the charge pump. In the locked state, we choose Ref (5MHz spur) or Ref/2 (2.5MHz spur) frequency comparison for charge pump; therefore the random clock can reduce and separate spurs in the frequency domain so as to accomplish a high performance PLL for communication.

B. Random clock generator

In Fig. 4, a new random clock generator and its presented. The spur at the reference frequency is reduced by operation are the factor of the number of the random clock bit length , which is directly related to the hardware cost, power consumption, and chip area. For the conventional random clock, it is likely to obtain more "1" than "0", which will degrade the suppression effect of the spur level. In this paper, the new random clock generator indicates that there are equal chances to get "0" and "1", which averages the periodic spur tones in the frequency domain. Fig. 4 illustrates that the Q1 has more chances to obtain "1" than "0", but the QN1, on the other hand, has more chances to obtain "0" than "1". Therefore, the MUX selection is to equalize the chance to get "1" and "0". The addition of the MUX selection can equivalently increase two more bits random clock generator. Therefore, the proposed circuit, as compared with the conventional 6-bit random clock generator occupies less area and consumes less power, especially which has the same function as the conventional 6-bit random clock. Effective bits for the new one achieve by adding a DFF and a MUX, it has less area and can save power, especially at high operation speed.

With reference clock period of T_{ref}, the traditional control voltage of the VCO can be simplified as [6]

$$r(t) = a_0 + \sum_{k=1}^{\infty} a_k \cos(\frac{k \times 2\pi}{T_{ref}})t \tag{2}$$

Consider the spur at the reference frequency, the corresponding term is

$$a_1 = \frac{1}{T_{ref}} \int_0^{Tref} r(t) \cos(\frac{2\pi}{T_{ref}} t)\, dt \tag{3}$$

Assume *p(t)* is the random-disturbing waveform with a period of mT_{ref}, where m is determined by the random bit length s, $m=2^s$. *p(t)* can be expressed as

$$p(t) = b_0 + \sum_{k=1}^{\infty} b_k \cos(\frac{k \times 2\pi}{m\, T_{ref}})t \tag{4}$$

Consider the random spur at the reference frequency, the corresponding term is

$$b_1 = \frac{1}{m\, T_{ref}} \int_0^{m\, Tref} p(t) \cos(\frac{2\pi}{T_{ref}} t)\, dt \tag{5}$$

P(t) can be expanded into n periodic pulses $S_1(t)$, $S_2(t)$,.....and $S_n(t)$ with the period of *mTref*. Each periodic pulse is the same, besides different phase shifts. Therefore we can rewrite (5) as

$$b_m = \sum_{k=1}^{n} c_{n,k} = \sum_{k=1}^{n} \frac{1}{mT_{ref}} \int_0^{mTref} s_k(t) \cos(\tfrac{2\pi}{T_{ref}} t)\, dt \tag{6}$$

According to the equation, the spur at the reference frequency is reduced by the factor of 2 to the power of the random clock bit length. Therefore, the spur power spectrum density can be averaged to accomplish a low-spur and smooth spectrum in the frequency domain.

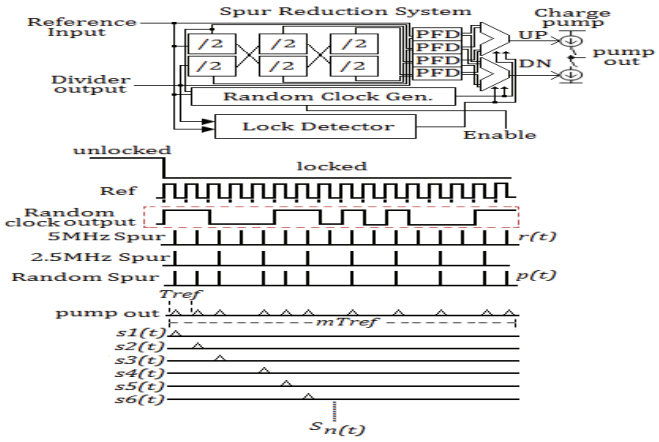

Fig.3. Spur reduction system.

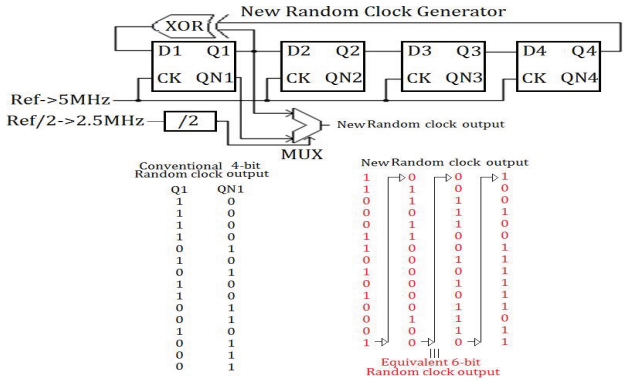

Fig.4. New random clock generator

C. Multi-Modulus Divider (MMD)

The choice of the divider architecture is essential for achieving low power dissipation and high design flexibility. One advantage of the MMD is that all the cells in the divider are identical, which can largely facilitate layout work. The programmable divider can provide an output signal with a period of:

$$T_{out} = (2^6 + B6 \cdot 2^5 + B5 \cdot 2^4 + B4 \cdot 2^3 + B3 \cdot 2^2 + B2 \cdot 2^1 + B1) \times T_{in}$$

This equation shows that the division ratios from 64 (if all CON=0) to 127 (if all CON=1) are achieved [7].

IV. Experimental Results

The circuit was designed and fabricated by TSMC 0.18-um 1P6M CMOS process. The low-spur frequency synthesizer has the output frequency range from 2.5GHz to 2.7GHz. The reference frequency is 5MHz. The tunable LC VCO range is from 2.2GHz to 2.8GHz, and the LC VCO gain is 336MHz/V. Without spur suppression mechanism, experimental results show the measured reference spur of -53dBc at 2.67GHz of locked frequency and -52dBc at 2.66GHz of locked frequency by 5MHz frequency offset. When the spur suppression circuit is enabled, the measured reference spurs are -72dBc and -73dBc, respectively, as shown in Fig 5. The Die micrograph is shown in Fig. 6. The area of the synthesizer is 1.56mm^2, include the LPF. The phase noise of -93dBc/Hz at 600 KHz offset and -112dBc/Hz at 3 MHz offset were obtained. The reduction amount of the reference spur in the entire tuning range is also illustrated in Fig 7. The proposed suppression technique has been implemented with 5MHz channel spacing for wireless application. Within the frequency range from 2.5GHz to 2.7GHz, the spur suppression levels are between 17dBc and 21dBc.

The performance summary and comparisons are provided in TABLE I and TABLE Π. This work has lower reference spur level, as compared with other 0.18um CMOS frequency synthesizers for wireless applications.

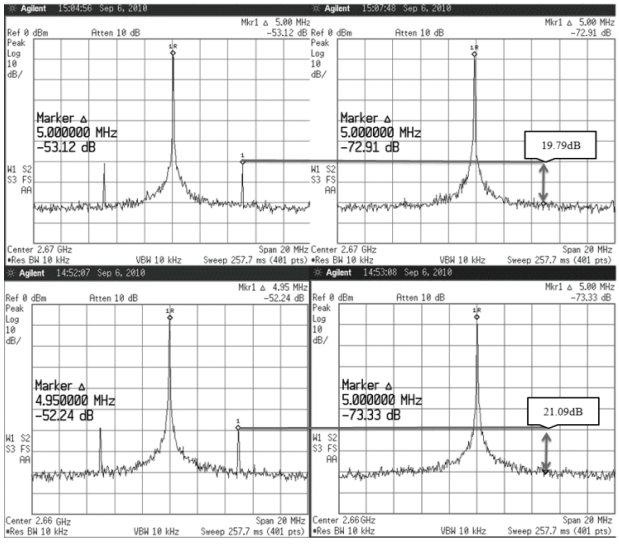

Fig.5. Measured spur reduction.

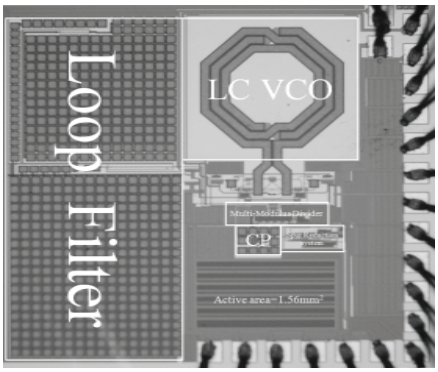

Fig.6. Die micrograph.

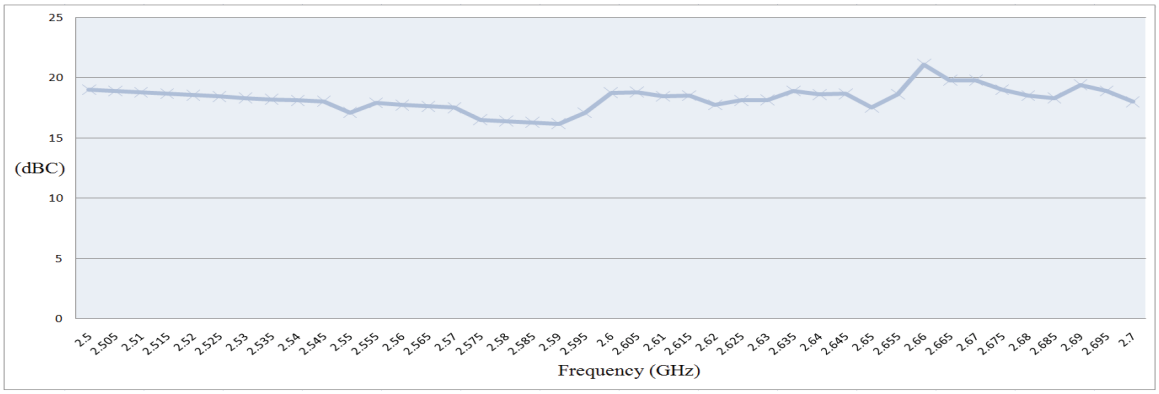

Fig.7. Measured spur suppression from 2.5GHz to 2.7GHz.

TABLE I. PERFORMANCE SUMMARY

Items	Performance
Technology	TSMC 0.18-um 1P6M CMOS
Power Supply	1.8V
Reference Fre.	5MHz
LC VCO	2.2GHz-2.8GHz
Divider ratio	500
Kvco	336MHz/V
Spur level	-72 dBc
Phase noise@600KHz	-93dBc/Hz
Phase noise@1MHz	-105dBc/Hz
Phase noise@3MHz	-111dBc/Hz
Power consumption	20mW

TABLE II. COMPARISON WITH PRIOR WORKS

	[4]	[8]	[9]	This work
Process	0.18um CMOS	0.25um CMOS	0.25um CMOS	0.18um CMOS
Supply	1.8	2.5v	2.5v	1.8
Power(mW)	18	13.5	117.5	20
Freq.	4.8/2.4 GHz	5.14-5.7GHz	4.12-4.72GHz	2.5-2.7 GHz
Ref. freq.	1MHz	10MHz	4MHz	5 MHz
Loop bandwidth	N/A	25KHz	90KHz	50KHz
Loop filter	2nd	3rd	N/A	3rd
Phase noise@1MHz(dBc/Hz)	-104/-110	-116	-87	-105
Ref. spur (dBc)	-55	-70	-45	-72

V. CONCLUSION

The low-spur frequency synthesizer, which randomizes the ripples on the VCO control voltage in order to reduce the reference spur at the output of the locked PLL, has been proposed. A new random clock generator is presented to perform the average operation. The circuit was implemented by TSMC 0.18-µm CMOS process and has achieved the phase noise of -93dBc/Hz at 600 KHz offset frequency and reference spurs below -72dBc.

ACKNOWLEDGMENT

The authors would like to thank National Chip Implementation Center for supporting the chip fabrication.

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