Definite Feature of Low-Energy Operation of Scaled Cross-Current Tetrode (XCT) SOI CMOS Circuits

Yasuhisa Omura and Daishi Ino
ORDIST and Grad. School of Scientific Eng., Kansai University
Suita, Osaka, Japan
Tel : +81-6-6368-1121
Fax : +81-6-6388-8843
e-mail : omuray@ipcku.kansai-u.ac.jp

Abstract - This paper introduces an advanced understanding of cross-current tetrode (XCT) CMOS devices and demonstrates their outstanding low-energy characteristics. An analysis of device operations reveals the aspect that will be enhanced at higher scaling levels. A simple analysis suggests that the low-energy operation of XCT CMOS devices stems from the potential floating effect yielded by the source diffusion of the original SOI MOSFET. It is strongly expected that this feature will be very useful in many medical implant applications in the future.

I Introduction

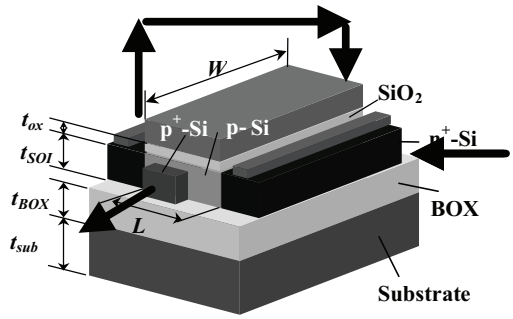
By using the partially-depleted (PD) single-gate (SG) SOI MOSFET, one of the authors (Omura) proposed the cross-current tetrode SOI MOSFET (XCT-SOI MOSFET) for analog applications (see Fig. 1) [1]. Though device modeling [2] and scaling feasibility [3, 4] of XCT-like devices have been studied recently, a detailed picture has not emerged because of the three-dimensionality of its operations. The feasibility of circuit applications of XCT-SOI CMOS has been investigated in order to exploit the potential of XCT devices [5]. Since the drivability of the XCT-SOI CMOS is about two-orders lower than that of the conventional SOI CMOS device [1, 2], the XCT-SOI CMOS is not attractive for high-speed applications. However, its suppression of short-channel effects and the almost zero degradation of the signal-to-noise ratio [4] appear very attractive for many digital and analog applications. Following this idea, we examined whether the XCT-SOI CMOS could provide low-energy operations [6]; the study highlighted its excellent potential.

As the device dimension in the previous study was not of the most recent scale, we advanced our consideration on the basis of the scaling scheme proposed in [4]. We demonstrated that scaling enhances the low-energy feature of the XCT-SOI CMOS [7]. Consequently, we can expect that XCT-SOI CMOS devices will yield new applications such as medical implant devices since they demand low-energy operation with high noise margin [8, 9].

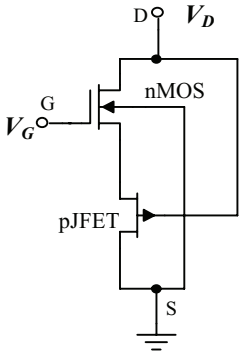
In order to discuss those applications in detail, device models for circuit simulations are necessary. The major part of recent considerations on low-energy circuits has been the subthreshold or near threshold characteristics of conventional CMOS devices. As is discussed in detail in [8, 10-12], the use of the above characteristics demands the proposal of new reliable device models suitable to circuit design and the degradation in the signal-to-noise ratio expected must be faced. On this point, the low-drivability of the XCT-SOI CMOS is based on the drift current and the reduced supply voltage in suppressing the energy dissipation. Therefore, new reliable device models are not needed and we think these features of the XCT-SOI CMOS offer great advantages to medical-implant applications and design methodology.

This paper considers how the energy dissipation of the XCT-SOI MOSFET can be suppressed by assuming an equivalent circuit model. Here we propose just such model to analyze the low-energy operation of XCT-SOI CMOS devices and circuits.

II. Device Structure and Assumptions for Modeling



(a) Bird's eye view of XCT device with parameter definitions and current flow. Arrows reveal the current flow.



(b) Equivalent circuit model of n-channel XCT-SOI MOSFET.

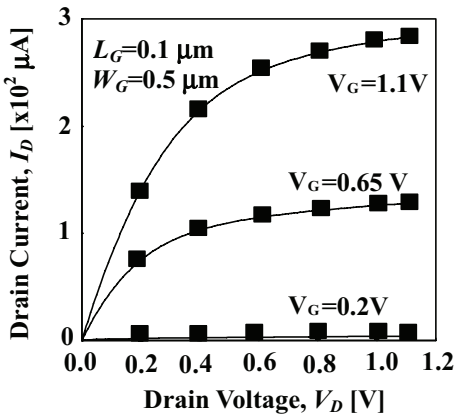
Fig. 1. XCT SOI MOSFET (bird's eye view and equivalent circuit model)

The schematic device structure is shown in Fig. 1. In an XCT structure, the n-channel MOSFET and p-channel JFET are self-merged and the electron current of the nMOSFET is relayed to the hole current of the pJFET in series [1]. The XCT device offers negative differential conductance (NDC) in the saturation region of the drain current [1, 2]. Since the

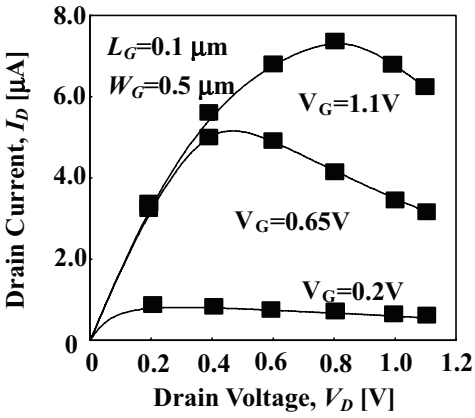
XCT device has active body contact, due to pJFET use, the body-floating effect is eliminated automatically.

In support of XCT-SOI MOSFET modeling, we have already proposed the equivalent circuit shown in Fig. 1(b) [1, 2, 5]. The basic availability of this model has been examined by circuit simulations [4-7]. However, the mechanisms underlying its low-power dissipation were not addressed in detail. In this paper, we discuss the dynamic operation of the XCT-SOI MOSFET to interpret its low-energy characteristic.

Before circuit simulations, we fabricated 2-μm gate XCT CMOS devices in order to characterize XCT devices in cooperation with Ricoh Corp. [2]. We extracted physical parameters from experimental results with the aid of 3-D device simulations [13]. Device parameters for deep sub-micron XCT devices were investigated based on above long-channel device simulation results; scaling scheme was also investigated [4]. Finally, physical parameters were applied to circuit simulations.



(a) Original nMOSFET



(b) XCT-SOI MOSFET

Fig. 2. I_D-V_D characteristics of original 0.1-μm-gate SOI MOSFET without parasitic JFET and XCT device. In (b), calculation results of those of 0.1-μm-gate nXCT-SOI MOSFET are also shown for comparison.

III. Device Simulation Results of SOI MOSFET and XCT-SOI MOSFET

First, we show the fundamental I_D-V_D characteristics of a 0.1-μm gate partially-depleted nMOSFET without the parasitic pJFET, see Fig. 2(a), following the 3-D device simulations in [13]; in the device simulations, the hydrodynamic transport model [14] and the quantum correction of electrostatic potential [15] are assumed. These devices are scaled down following the specific scheme suitable for XCT devices [4]. Device parameters assumed here are summarized in Table I. Since the nMOSFET has a body tie, it does not suffer from the kink phenomenon of drain current. It does, however, show slight short-channel effects due to channel length modulation.

Figure 2(b) shows the I_D-V_D characteristics of an nXCT-SOI MOSFET with a 0.1-μm-long gate as determined from 3-D device simulations. It is seen that the XCT device has lower I_D than the MOSFET because of the series resistance of the parasitic pJFET. In addition, the XCT device exhibits negative differential conductance [1]. On the other hand, the short-channel effects (SCEs) of the original MOSFET are well suppressed in the XCT device; subthreshold swing is 76 mV/dec at V_D=1V. This is one of the great advantages of XCT devices.

TableI. Device parameters assumed in simulations

	N_A [cm^{-3}]	L_G [μm]	t_{ox} [nm]	t_{SOI} [nm]	t_{BOX} [nm]	V_D [V]	V_{TH} (*) [V]
Scaling Scheme	k	1/k	4/3k	1/k$^{1/3}$	1/k$^{1/3}$	1/k$^{1/2}$	---
k=2	1e17	1.0	20	278	238	3.5	0.58
k=20	2e18	0.1	2.0	129	111	1.10	0.10

(*) n$^+$-poly-Si gate is assumed.

IV. XCT-CMOS Device and Circuit Characteristics

A. Power dissipation and delay of XCT-SOI CMOS

First, we simulated the dissipation power (P_d) and delay time (t_d) of the conventional SOI CMOS EXOR and XCT-SOI CMOS EXOR with a 1.0-μm-long gate or a 0.1-μm-long gate; device parameters were extracted with the aid of a device simulator [13, 16], and 10 EXOR chains were assumed. Each EXOR is composed of 6 CMOS inverters. Simulation results of P_d are shown as a function of supply voltage (V_{DD}) in Fig. 3; in Fig. 3(a), simulation results of 1-μm-long gate devices are shown, and in Fig. 3(b), simulation results of 0.1-μm-long gate devices are shown.

The XCT-SOI CMOS EXOR composed of 1-μm-long gate devices reveals lower power consumption than the conventional SOI CMOS EXOR. On the other hand, the XCT-SOI CMOS EXOR with 0.1-μm-long gate devices offers a power consumption that is 2 orders lower than that of the conventional SOI CMOS EXOR because the drain current level of the XCT-SOI MOSFET is about 2 orders lower than that of the original SOI MOSFET as already described. In addition, the conventional SOI CMOS with a 0.1-μm-long gate suffers from high subthreshold leakage due to the short-channel effect, while the XCT-SOI CMOS is almost free from the short-channel effect in spite of the identical threshold voltage. In Fig. 3(b), it is assumed that both the n-channel SOI MOSFET and n-channel XCT-SOI MOSFET have the threshold voltage (V_{THn}) of 0.1 V and both the p-channel SOI MOSFET and p-channel XCT-SOI MOSFET have the threshold voltage (V_{THp}) of -0.1 V. Since the performance comparison shown in Fig. 3(b) is not appropriate, we raised the threshold voltage values of the SOI MOSFET and the

XCT-SOI MOSFET; V_{THn}= 0.2 V and V_{THp}= -0.2 V. Simulation results of P_d are shown as a function of V_{DD} in Fig. 3(c). The XCT-CMOS EXOR composed of 0.1-μm-long gate devices still offers a power consumption that is about 50 times lower than that of the conventional SOI CMOS EXOR.

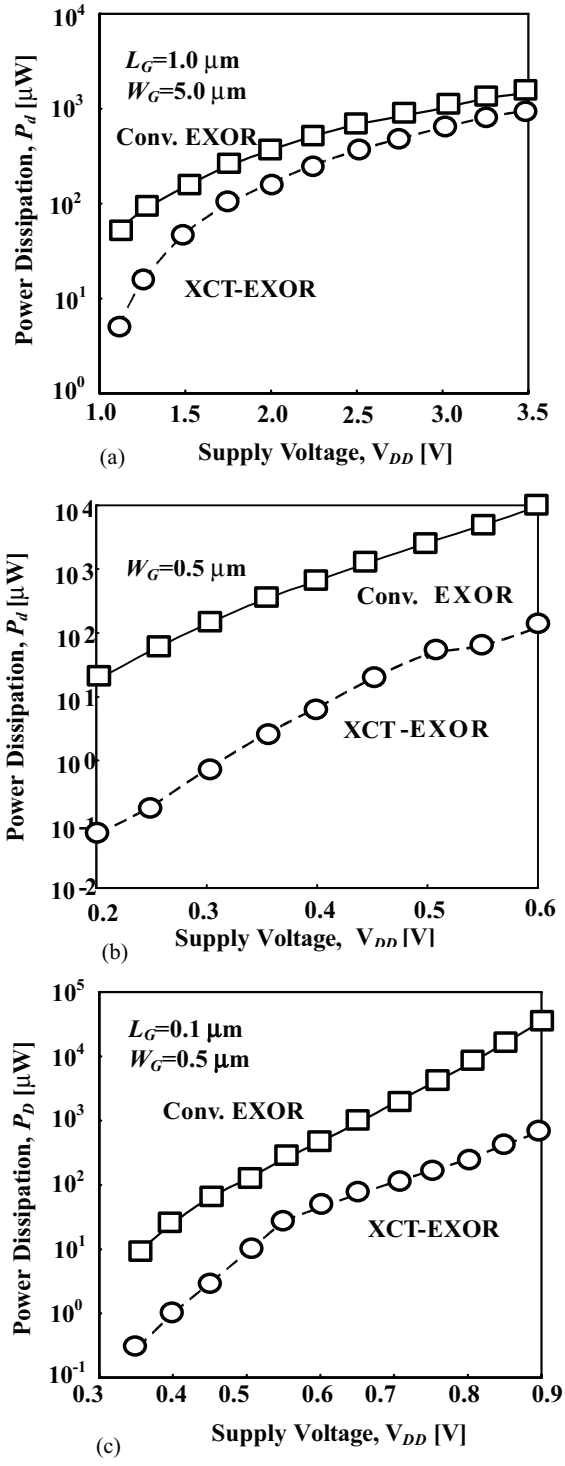


Fig. 3. Simulated power dissipation characteristics for L_G= 1.0 μm and 0.1 μm. The vertical axis is normalized by the total number of EXOR units. 1-μm-long gate CMOS (V_{THn}=0.58 V and V_{THp}= -0.58 V), (b) 0.1-μm-long gate CMOS (V_{THn}=0.1 V and V_{THp}= -0.1 V), (c) 0.1-μm-long gate CMOS (V_{THn}=0.2 V and V_{THp}= -0.2 V).

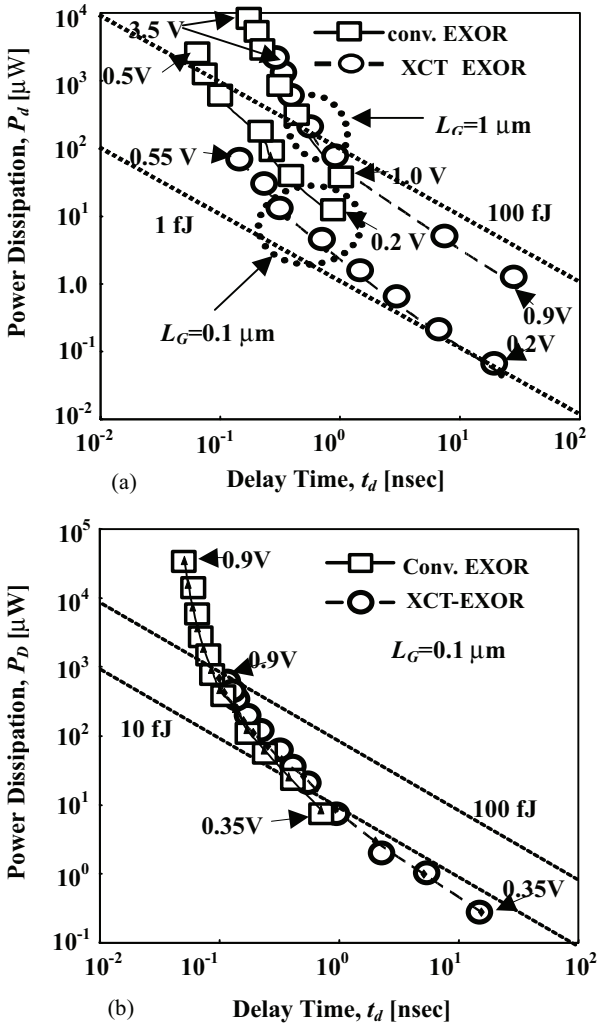


Fig. 4. Simulated P_d vs t_d characteristics for L_G= 1.0 μm and L_G= 0.1 μm. The vertical axis is normalized by the total number of EXOR units. (a) It is assumed that the threshold voltage of 0.1-μm-long gate device is 0.1 V for nMOS and -0.1 V for pMOS, (b) It is assumed that the threshold voltage of 0.1-μm-long gate device is 0.2 V for nMOS and -0.2 V for pMOS.

Figure 4 reveals P_d vs. t_d characteristics of 0.1-μm- and 1-μm-gate XCT-SOI CMOS EXOR, where those of the conventional SOI CMOS EXOR are also shown for comparison. Following the scaling scheme proposed in [4], the original SOI nMOSFET and pMOSFET suffer from the short-channel effects and slightly high leakage currents. The original SOI MOSFETs in Fig. 4(a) were implemented as an CMOS inverter without any adjustment of the threshold voltage; the conventional SOI CMOS reveals a higher dissipation energy than the XCT-SOI CMOS. In Fig. 4(b), on the other hand, the threshold voltages of the original SOI nMOSFET and original SOI pMOSFET are assumed to be 0.2 V and -0.2 V, respectively, to suppress the subthreshold leakage current.

First we consider the case shown in Fig. 4(a). In the case of the 1-μm-gate CMOS, the delay time of XCT-EXOR is one order greater than that of the conventional CMOS EXOR, and the product of P_d and t_d is almost identical. In the case of the 0.1-μm-gate CMOS, however, the product of P_d and t_d is, for the XCT-EXOR, one order lower than that of the conventional

CMOS EXOR. It is made clear from the device simulation results that the conventional CMOS EXOR suffers from short-channel effects; this results in a high leakage current and high energy dissipation. The XCT-EXOR, on the other hand, is almost free from short-channel effects and can minimize the energy dissipation. This is the greatest advantage of the XCT-EXOR. Next, we address the case shown in Fig. 4(b). In the case of the 0.1-μm-gate CMOS, the product of P_d and t_d is, for the XCT-EXOR, roughly the same as that of the conventional CMOS EXOR. This appears to suggest that the XCT-EXOR may not exhibit substantially lower energy operation than the conventional SOI CMOS EXOR, but this is contradicted below.

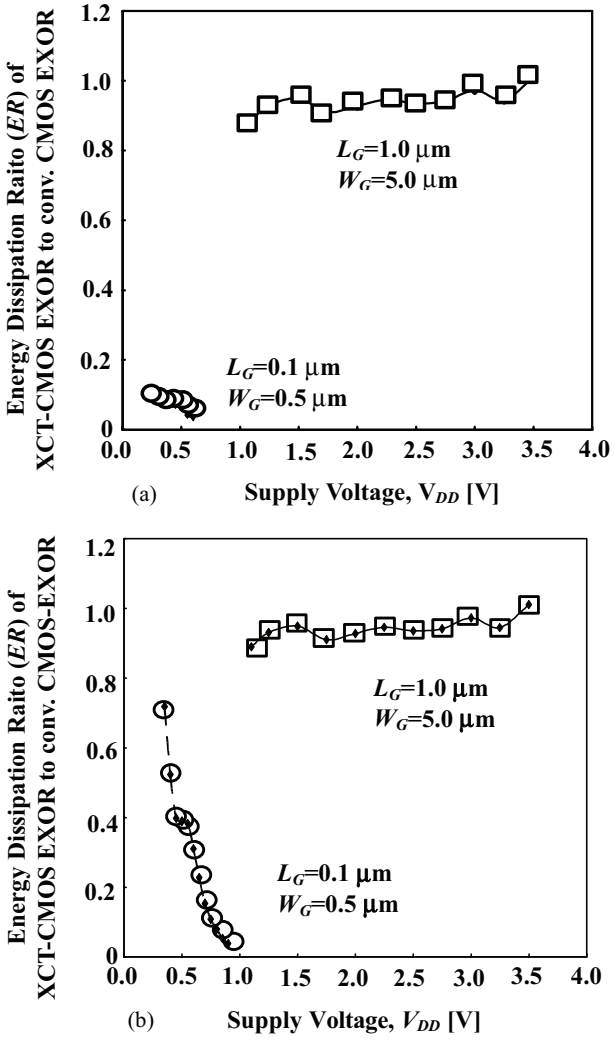


Fig. 5. Calculation results of energy ratio (*ER*) of the energy dissipation of 1.0-μm-long gate CMOS EXOR and 0.1-μm-long gate CMOS EXOR. The energy ratio is defined with the energy dissipated by the XCT-EXOR divided by that of the conventional CMOS EXOR. (a) *ER* for data shown in Fig. 4(a), (b) *ER* for data shown in Fig. 4(b). The data for 1-μm-long gate devices are the same as those in Fig. 4(a).

B. Low-Energy Advantage of XCT-SOI CMOS

In the previous section, we revealed that the scaled XCT-EXOR may have much lower energy dissipation than the conventional SOI CMOS EXOR. Here we advance the discussion to deepen the understanding of XCT-EXOR features. We concentrate the discussion on the energy ratio of CMOS-EXOR circuits, where energy ratio (*ER*) is defined as the energy dissipated by the XCT-EXOR divided by that of the comparable conventional SOI EXOR. Calculation results are shown in Fig. 5; Figure 5(a) corresponds to the devices shown in Fig. 4(a) and Figure 5(b) to the devices shown in Fig. 4(b).

In Fig. 5(a), first, it is seen that the *ER* value of 1-μm-long gate devices is almost unity regardless of the assumed V_{DD} value. This behavior is reasonable for the following reasons. The energy dissipation of conventional devices, evaluated by the P_d-t_d product, is not a function of V_{DD} due to the simple recognition of the MOS gate capacitor's charging and discharging operations. It is anticipated that the XCT-CMOS with 1-μm-long gate follows this principle. In the case of 0.1-μm-long gate devices, on the other hand, it is seen that the *ER* value is much less than unity for all assumed V_{DD} values. We can't conclusively state that this behavior is reasonable because the conventional CMOS devices are somewhat leaky due to the short-channel effect. Our solution was to recalculate the ER data following the data shown in Fig. 4(b); in Fig. 5(b), the conventional SOI CMOS does not have any leakage current due to the short-channel effect. It should be noted that the *ER* rapidly falls as V_{DD} rises. Since this is a very interesting result and somewhat mysterious, we discuss a possible mechanism based on physics in the next section.

V. Discussion on Dynamic Operation of XCT devices

As the parasitic pJFET works like a resistor connected to the source terminal of the MOSFET, we propose a possible model for *AC* analysis of the XCT-SOI MOSFET in Fig. 6, where $C_{Gn,MOS}$ denotes the gate-to-source capacitance of an n-channel SOI MOSFET, $R_{ch,pJFET}$ denotes the effective resistance of pJFET channel, and $C_{Sn,BOX}$ and $C_{Dn,BOX}$ mean the parasitic capacitances below the source and the drain diffusions, respectively. This model yields the following expressions of parasitic components. The effective gate capacitance ($C_{Gn,XCT}$) of the n-channel XCT-SOI MOSFET is given by

$$C_{Gn,XCT} = \frac{C_{Gn,MOS}\left(1+(\omega C_{Sn,BOX}R_{ch,pJFET})^2\right)}{1+\omega^2 C_{Sn,BOX}(C_{Sn,BOX}+C_{Gn,MOS})R_{ch,pJFET}^2}. \quad (1)$$

In a similar manner, we have the following effective gate capacitance ($C_{Gp,XCT}$) of a p-channel XCT-SOI MOSFET.

$$C_{Gp,XCT} = \frac{C_{Gp,MOS}\left(1+(\omega C_{Sp,BOX}R_{ch,nJFET})^2\right)}{1+\omega^2 C_{Sp,BOX}(C_{Sp,BOX}+C_{Gp,MOS})R_{ch,nJFET}^2}, \quad (2)$$

where $C_{Gp,MOS}$, $C_{Sp,BOX}$, and $R_{ch,nJFET}$ are the counterparts of the n-channel XCT-SOI MOSFET components. The angular frequency ($\omega=2\pi/\tau_d$) is a function of V_{DD}.

From these expressions, when it is assumed that the energy dissipation of the device stems only from the charging and discharging processes of the gate capacitance, the total energy (E_{XCT} and E_{CC}) is equivalent to the product of P_d and t_d and is approximately given as

$$E_{XCT}(\omega) = (C_{Gn,XCT} + C_{Gp,XCT} + C_{Dn,BOX} + C_{Dp,BOX})V_{DD}^2, \quad (3)$$

for the XCT-SOI CMOS and

$$E_{CC} = (C_{Gn,MOS} + C_{Gp,MOS} + C_{Dn,BOX} + C_{Dp,BOX})V_{DD}^2, \quad (4)$$

for the conventional SOI CMOS. Thus their ratio ($ER=E_{XCT}/E_{CC}$) is expressed as

$$ER(\omega) = \frac{C_{Gn,XCT} + C_{Gp,XCT} + C_{Dn,BOX} + C_{Dp,BOX}}{C_{Gn,MOS} + C_{Gp,MOS} + C_{Dn,BOX} + C_{Dp,BOX}}. \quad (5)$$

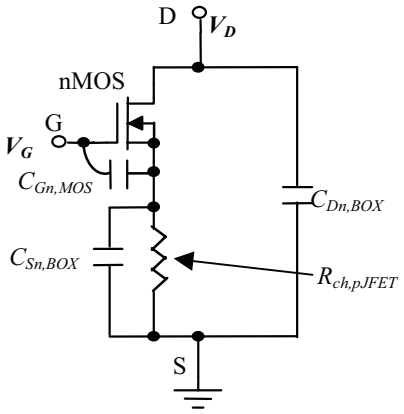


Fig. 6. A possible model for AC analysis of n-channel XCT-SOI MOSFET.

Assuming that $R_{ch,pJFET}=R_{ch,nJFET}$, $C_{Gp,MOS}=2C_{Gn,MOS}$, $C_{Sn,BOX}=C_{Dn,BOX}$, and $C_{Sp,BOX}=C_{Dp,BOX}$, we plot *ER* values as a function of the scaling factor (k) in Fig. 7. *ER* values are plotted as a parameter of frequency ($f=1/\tau_d$). Generally speaking, reducing the gate length (L_G) raises the operation frequency at the same supply voltage. In Fig. 7, the *ER* rises when the scaling factor (k) increases; this is because the present scaling scheme [3] slightly reduces $C_{Sn,BOX}R_{ch,pJFET}$ and $C_{Sp,BOX}R_{ch,nJFET}$. For $f< 1/(C_{Sn,BOX}R_{ch,pJFET})$ and $f<1/(C_{Sp,BOX}R_{ch,nJFET})$, the role of $C_{Sn,BOX}$ and $C_{Sp,BOX}$ is lost; *i.e.*, we have $C_{Gn,XCT}\sim C_{Gn,MOS}$ and $C_{Gp,XCT}\sim C_{Gp,MOS}$. As a result, the *ER* value approaches unity when k increases; the intrinsic advantage of the XCT-SOI CMOS is lost. For $f > 1/(C_{Sn,BOX}R_{ch,pJFET})$ and $f > 1/(C_{Sp,BOX}R_{ch,nJFET})$, on the other hand, we have $C_{Gn,XCT}<C_{Gn,MOS}$ and $C_{Gp,XCT}<C_{Gp,MOS}$. In this case, the *ER* value decreases as the frequency rises. In order to have a small *ER* value, we have to increase the effective channel resistance of the parasitic JFET as scaling is advanced. As shown in Fig. 7, for f= 10 GHz, the *ER* value is very low over a wide range of k. The dotted arrows reveal the lowest-to-highest range of supply voltage applicable to the 1-μm-long gate CMOS (for k= 1) and the 0.1-μm-long gate CMOS (k= 20). The dotted arrows suggest that the energy dissipation of a scaled XCT-SOI CMOS can be well reduced at the highest V_{DD} values applicable to the scaled device. Consequently, we can conclude that the potential floating effect of the source diffusion of the SOI MOSFET plays an important role in reducing the energy dissipated by XCT-CMOS devices. In the case of the 1-μm-long gate CMOS, however, the calculated *ER* value based on Eq. (5) fails to match the circuit simulation result. It is suggested that the potential floating effect of the source diffusion is overestimated in the above model; in other words, the effective channel resistance of the parasitic pJFET is overestimated.

From the above considerations, the important features of the scaled XCT-SOI device are summarized as follows:

(1) Low-energy operation is possible without lowering the supply voltage.

(2) As a low supply voltage is not needed to reduce the current level in circuit design, the signal-to-noise ratio is not degraded assuming voltage-drive logic.

(3) Low-energy operation is realized without assuming subthreshold or near-threshold operation.

(4) The conventional design scheme can basically be applied to low-energy circuit designs.

(5) The negative differential conductance of XCT-SOI device contributes to the realization of the above features by suppressing the short-channel effect.

(6) The potential floating effect of XCT devices is the key factor in reducing energy dissipation.

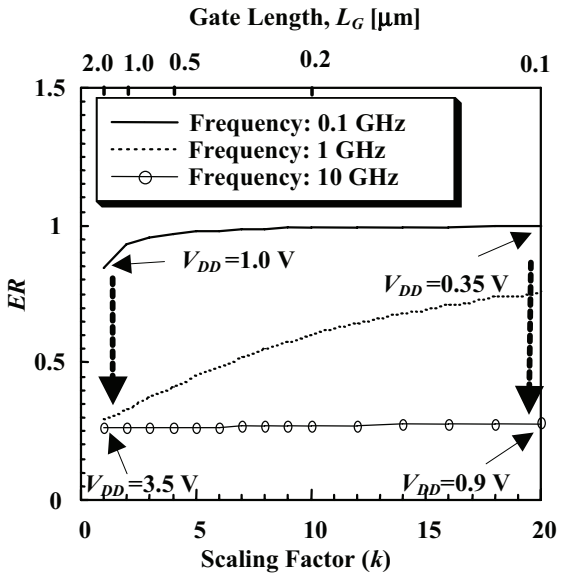


Figure 7. Dissipated energy ratio as a function of the scaling factor. It is assumed that the energy dissipation consists only of the charging and discharging processes of the gate capacitor. Scaling scheme is described in [3]. The dotted arrows reveal the lowest-to-highest range of supply voltage applicable to 1-μm-long gate CMOS (for k= 1) and 0.1-μm-long gate CMOS (k= 20).

VI. Summary

We demonstrated the low-energy operation of scaled XCT-SOI CMOS devices and analyzed the underlying mechanism. It was shown that the source-follower like operation of XCT-SOI MOSFET reduces the effective input capacitance, and thus the dissipated energy of the XCT-SOI device. Therefore, XCT-SOI CMOS is a very promising device for various low-energy circuits.

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References

[1] Y. Omura and K. Izumi, “High-gain Cross-current Tetrode MOSFET/SIMOX and Its Application”, in Ext. Abstr., 18th Int. Conf. Solid State Devices and Mat. (Tokyo, 1986) p. 715.

[2] Y. Azuma, Y. Yoshioka, and Y. Omura, “Cross-Current SOI MOSFET Model and Important Aspects of CMOS Operations,” Ext. Abstr. Int. Conf. Solid State Devices and Mat. (Tsukuba, Sept. 2007) pp. 460-461.

[3] B. J. Blalock, S. Cristoloveanu, B. M. Dufrene, F. Allibert, and M. Mojarradi, “The Multiple-gate MOSFET-JFET Transistor”, Int. J. High Speed Electron. Syst., vol. **12**, pp. 511-520, 2002.

[4] Y. Omura, K. Fukuchi, D. Ino, and O. Hayashi, “Scaling Scheme and Performance Perspective of Cross-Current Tetrode (XCT) SOI MOSFET for Future Ultra-Low Power Applications”, Proc. 15th Int. Symp. Semiconductor-on-Insulator Technol. and Related Phys. (219th ECS meet., Montreal, 2011) vol. **35**, No. 5, pp. 85-90.

[5] Y. Omura, “Cross-Current Silicon-on-Insulator Metal-Oxide Semiconductor Field-Effect Transistor and Application to Multiple Voltage Reference Circuits,” Jpn. J. Appl. Phys., vol. **48**, pp. 04C07-04C11, 2009.

[6] S. Tominaga and Y. Omura, “Sub-circuit SPICE Model of Cross-Current Tetrode (XCT) SOI MOSFET and Analysis of Low-power XCT CMOS Operation”, Abstr. 2009 IEEE Int. Meet. Future of Electron Devices, Kansai, pp. 116-117.

[7] D. Ino and Y. Omura, “Scaling Study of Cross-Current Tetrode (XCT) SOI MOSFET for Future Ultra-Low Energy Applications ”, Abstr. 2011 IEEE Int. Meet. Future of Electron Devices, Kansai, pp. 54-55.

[8] A. P. Chandrakasan, D. C. Daly, D. F. Finchelstein, J. Kwong, Y. K. Ramadass, M. E. Sinangil, V. Sze, and N. Verma, “Technologies for Ultradynamic Voltage Scaling”, Proc. the IEEE, vol. 98, pp. 191-214, 2010.

[9] M. Koyanagi, Y. Nakagawa, K. Lee, T. Nakamura, Y. Yamada, K. Inamura, K. Park, K. Kurino, “Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology”, Proc. IEEE Int. Solid-St. Cur. Conf. (ISSCC) (San Francisco, Feb, 2001) pp. 270-271.

[10] D. Markovic, C. C. Wang, L. P. Alarcon, T.-T. Liu, and J. M. Rabaey, “Ultralow-Power Design in Near-Threshold Region”, *Proc. IEEE,* 98 (2010) pp. 237-252.

[11] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, “Near-Threshold Computing: Reclaiming Moore’s Law Through Energy Efficient Integrated Circuits”, *Proc. IEEE,* 98 (2010) pp. 253-266.

[12] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, “FDSOI Process Technology for Subthreshold-Operation Ultralow-Power Electronics”, *Proc. IEEE,* 98 (2010) pp. 333-342.

[13] Sentaurus Users Manual, Synopsys, 2008.

[14] H. Nakajima, S. Yanagi, K. Komiya and Y. Omura, "Off-leakage and draive current characteristics of sub-100-nm SOI MOSFETs and impact of quantum tunnel current," IEEE Trans. Eletron Devices, vol. 49, No. 10, pp. 1775-1782, 2002.

[15] G. Paasch and H. Uebensee, “A Modified Local Density Approximation –Electron Density in Inversion Layers-”, Phys. Status Solidi B vol. **113**, pp. 165-178, 1982.

[16] HSPICE Users Manual, Synopsys, 2008.