Electro-Thermal Modeling and Reliability Simulation of Power MOSFETs with SystemC-AMS － Case Study: An Unclamped Inductive Switching Test Circuit

Keiji Nakabayashi†, Takahiro OZASA†, and Tamiyo Nakabayashi‡

†Keirex Technology Inc.
1-1-26 Irifune, Nagai Bldg, Chuo-ku, Tokyo, Japan
{nakabayashi.keiji, ozasa}@keirex.com

‡Nara Women's University
Kitauoyahigashi-machi, Nara, Japan
nakaba@ics.nara-wu.ac.jp

Abstract

We present a new technique for the electro-thermal modeling and reliability simulation of power MOSFETs with SystemC-AMS. We model the non-linear electrical characteristics and self-heating effect of the power MOSFETs, and improve a numerical integration method in order to solve numerical instability of SystemC-AMS. Our technique is verified by experimental results using an Unclamped Inductive Switching (UIS) test circuit.

I. Introduction

SystemC is a standardized C++ based library which is used for the modeling and simulation of large digital hardware/software systems on high abstraction levels. SystemC-AMS extends SystemC for modeling of analog/mixed-signal (AMS) systems and mixed-level heterogeneous systems [19].

The 1.0 beta2 version (is a latest version at the time of this writing) of SystemC-AMS provides the models of computation (MoC), which are composed of TDF (Timed Data Flow), LSF (Linear Signal Flow), and ELN (Electrical Linear Networks) [19]. The TDF MoC is used for the discrete-time domain modeling of linear and/or non-linear functional blocks. The LSF MoC is used for the continuous-time domain modeling of linear systems such as a set of linear algebraic equations. The ELN MoC is used for the continuous-time domain modeling of linear electrical networks [19]. SystemC-AMS provides two solvers. One is the TDF solver that supports the TDF MoC, and the other is the linear differential algebraic equations (DAE) solver that supports the ELN MoC and the LSF MoC. The whole system is solved using these two solvers simultaneously [19].

We briefly review previous main research activities with respect to the application of SystemC-AMS. In the research of [9], SystemC-AMS is used for the system level modeling, simulation, and verification of digital protection functions of smart power switches that are composed of a digital controller and a power MOSFET. In the researches of [1], [7], [12], and [14]-[15], SystemC-AMS is used to model and simulate the behaviours of AMS systems and RF analog systems. Particularly, in comparison in terms of simulation run-time with hardware description language VHDL-AMS, VHDL-AMS simulator ran about 10 times faster than SystemC-AMS [12]. Furthermore, in the research of [2], SystemC-AMS is used to model and simulate DC-DC converters on system level. In the comparison with other modeling/simulation tool, SystemC-AMS ran about 10 times faster than MATLAB/Simulink.

On the other hand, in the research of [8], SystemC-AMS is applied to the analysis of a heterogeneous system. The physical control system that is composed of a crane and its controller is modelled and simulated with SystemC-AMS. In the researches of [4] and [6], SystemC-AMS is applied to multi-physics (multiple physical domains) modeling and its simulation. For example, recent work [4] models a harvester of vibration energy with SystemC-AMS. The system of the harvester of vibration energy is composed of mechanical, electro-mechanical, and electrical subsystems.

As described above, previous main research activities with respect to the application of SystemC-AMS have handled system level modeling and simulation of AMS systems, heterogeneous systems, and multi-physics, and so on.

The aim of our research is to propose a new technique for the simple electro-thermal device level modeling and reliability simulation of power MOSFETs (MOSFETs) with SystemC-AMS. As a case study, we focus on an Unclamped Inductive Switching (UIS) test circuit which is used for an avalanche breakdown test of the MOSFET. The avalanche breakdown is affected by the device junction temperature rise that is due to self-heating of the MOSFET. In the reliability simulation, it is essential that the coupling of the electrical domain and thermal domain (electrical-thermal coupling) is considered.

In our study, first, we consider a non-linear current-voltage characteristic (I-V characteristic) of the

power MOSFET. We model the characteristic as a voltage-controlled resistor (on/off switching resistance) and express its equation by using the TDF MoC. The resistor value is updated in each simulation time step (time step). The resistor is incorporated into an electrical linear network which is expressed by ELN. Thus, we are able to simulate the electrical network which includes the non-linear MOSFET with SystemC-AMS. And, we enable the electro-thermal reliability simulation by coupling a thermal network that expresses thermal conduction in the MOSFET. Next, we consider the switching behaviours with steep signal changes (steep switching) of the UIS test circuit. Since the TDF MoC has discrete-time domain, we set simulation time step (time step) interval small so that that it is as equal as possible to continuous-time domain. Thus, we are able to deal with simulation of the steep switching circuit.

Furthermore, we improve a numerical integration method in order to solve numerical instability issues [8] that are due to the DAE solver of SystemC-AMS. Finally we verify our technique in the comparison with previous SPICE electro-thermal simulation of [10]-[11].

In the next section, we explain an Unclamped Inductive Switching (UIS) test circuit. Section III describes a previous SPICE electro-thermal power MOSFET model. Section IV describes our SystemC-AMS electro-thermal power MOSFET model and simulation technique. Section V describes our experiments and compares the results. We conclude the paper in Section VI.

NOMENCLATURE

T_{nom}	Room temperature [K]
β	MOSFET channel conductance [A/V^2]
β_0	Value of β at T_{nom} [A/V^2]
V_{th}	Threshold voltage [V]
V_{th0}	Value of V_{th} at T_{nom} [V]
V_{gs}	Gate-source voltage [V]
V_{ds}	Drain-source voltage [V]
C_{gs}	Gate-source capacitance [F]
C_{ds}	Drain-source capacitance [F]
C_{gd}	Gate-drain capacitance [F]
$R_{ds(on)}$	Drain-source on resistance [Ohm]
$R_{ds(off)}$	Drain-source off resistance [Ohm]
R_{ds}	Drain-source resistance [Ohm]
I_{ds}	Drain-source current [A]
TCV_{th}	Temperature coefficient of V_{th} [1/K]
$TC\beta$	Temperature coefficient of β [-]
BV_{dss}	Avalanche breakdown voltage [V]
$BV_{dss(eff)}$	Effective avalanche breakdown voltage [V]
R_{body}	Body resistance [Ohm]
T_h	Thermal node [-]
$V(T_h)$	Nodal Voltage at T_h [V]
V_{dd}	Power supply voltage [V]
V_{pulse}	Pulse voltage source [V]
V_{mnt}	Voltage source for current monitor [V]
$I(V_{mnt})$	Monitored current [A]
V(DRAIN,SOURCE)	Drain-source voltage [V]
L_{drain}	Drain load inductance [H]
R_{drain}	Drain load resistance [Ohm]
R_{gate}	Gate resistance [Ohm]
T_j	Device junction temperature [K]
T_{case}	Case temperature [K]
T_{amb}	Ambient temperature [K] (T_{amb}= T_{nom})
V_{amb}	Ambient temperature definition [K]
G_{mos_pwr}	Power dissipation [W]
C_{thp}	Case-ambient thermal capacitance [J/K]
R_{thp}	Case-ambient thermal resistance [K/W]
B_j	Device junction temperature transform [-] (temperature feedback: $V(T_h)$= T_j)

II. Unclamped Inductive Switching Test Circuit

An UIS test circuit is used to evaluate tolerance for the avalanche breakdown that is the most important reliability assessment of a power MOSFET. Figure. 2. 1 depicts the schematic of the UIS test circuit that is used in [10]-[11]. Basically, the UIS test circuit is a steep switching circuit that is composed of the MOSFET as a switch, and a parasitic inductor as a load. The counter electromagnetic force that is induced by the inductance causes a significant over voltage transient between drain and source of the MOSFET. If the resulting voltage transient is large enough, the MOSFET is forced into drain-source avalanche breakdown. And the high drain-source current causes its device junction temperature rise that is due to self-heating effect. The device junction temperature rise affects the avalanche breakdown voltage and electrical characteristics of the MOSFET.

In other words, it is very important that the device junction temperature rise that is due to self-heating effect is reflected to the MOSFET characteristics. In the UIS test circuit, particularly, on/off switching resistance (drain-source resistance) and avalanche breakdown of the MOSFET are important characteristics, which have temperature dependence.

Therefore, the electro-thermal device model that incorporates with self-heating effect and the electrical characteristics is essential in the UIS test circuit simulation for tolerance evaluation of the avalanche breakdown [10]-[11], [16], [18], [20].

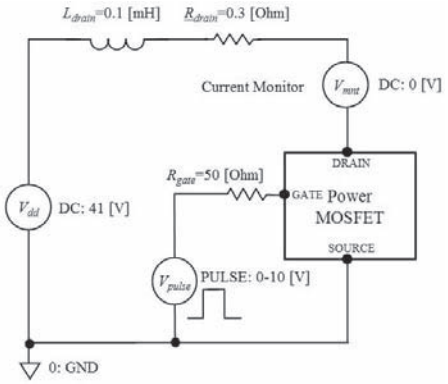


Fig. 2.1: Unclamped Inductive Switching test circuit of [10]-[11].

III. Previous SPICE Electro-Thermal Power MOSFET Model

We use the SPICE electro-thermal power MOSFET model of [10]-[11] as a reference. In the study of [10]-[11], it is reported that the SPICE simulation results with the model correspond to the measurement results of the UIS test circuit that is depicted in Fig. 2. 1. Therefore, in our study, we use the model and its SPICE simulation results as comparison data. The model is given as a subcircuit of PSPICE (a PC version of SPICE) [10]-[11].

We briefly review the SPICE electro-thermal power MOSFET model of [10]-[11] that are depicted in Fig. 3. 1 and Fig. 3. 2. The model is composed of an electrical equivalent circuit model (Fig. 3. 1) and a thermal equivalent circuit model (Fig. 3. 2).

The electrical characteristics and power dissipation ($G_{\mathrm{mos\_pwr}}$) of the MOSFET are calculated by using the electrical equivalent circuit model. The power dissipation flows into the thermal equivalent circuit model as a current source, and the device junction temperature (T_j) is calculated as a nodal voltage. The device junction temperature is fed back to the electrical equivalent circuit model as nodal voltage ($V(T_h)$) of thermal node (T_h). Then the values of very important parameters with (device) temperature dependence such as threshold voltage, channel conductance, (effective) avalanche breakdown voltage, and so on are updated. Based on the updated values, next computation process goes. A series of computation processes is repeated at each time step in electro-thermal simulation. Note that the thermal equivalent circuit model is a linear network that composed of thermal resistances and thermal capacitances, which expresses thermal conduction from device junction (node T_j) to package case (node T_{case}) [1].

On the other hand, the electrical equivalent circuit model very accurately express current-voltage characteristic (I-V characteristic) of the MOSFET. Then its AC characteristics are modelled as an input capacitance, an output capacitance, and a feedback capacitance (internal capacitive feedback). Its body diode and reverse recovery time are expressed as one SPICE diode model. Its drain-source avalanche breakdown and effective breakdown voltage are expressed as a series connection of the other SPICE diode model and a effective breakdown voltage source. Furthermore, it models temperature dependence of threshold voltage, channel conductance and so on with using temperature coefficients.

As described above, the model of [10]-[11] is very accurate, but is very complex. Due to its complexity, it is pointed out that non-convergence can occur [10]-[11].

[1] The thermal conduction from package case to ambient is expressed as a linear circuit that compose of a thermal resistance and a thermal capacitance. We discuss the circuit in the Section V.

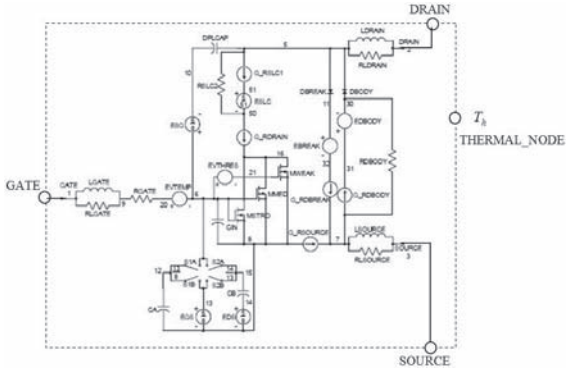


Fig. 3.1: electrical equivalent circuit model of electro-thermal power MOSFET model of [10]-[11].

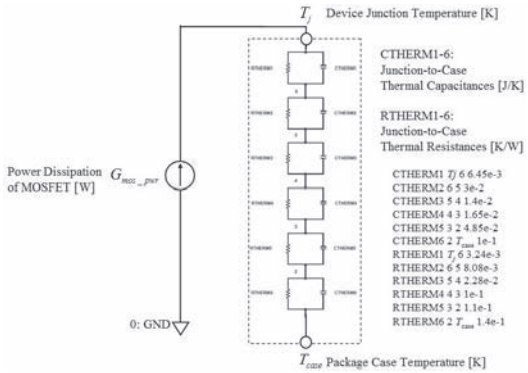


Fig. 3.2: thermal equivalent circuit model of electro-thermal power MOSFET model of [10]-[11].

IV. Our SystemC-AMS Electro-Thermal Power MOSFET Model

We need new techniques to model non-linear devices such as a power MOSFET and a diode, and to handle an UIS test circuit with steep switching by SystemC-AMS. First we describe our SystemC-AMS electrical power MOSFET model (our SystemC-AMS power MOSFET model).

We use the TDF MoC of SystemC-AMS in order to describe the characteristics and/or functional behaviours of non-linear devices. Figure 4. 1 depicts a method of non-linear I-V characteristic modeling of the power MOSFET. The characteristic equation of the MOSFET is expressed with using the TDF Moc, and is connected into the ELN MoC with using ELN modules.

As described in Section I, The TDF MoC has discrete-time domain, and the ELN MoC has continuous-time domain. Then the TDF solver and the DAE solver that support the ELN MoC run simultaneously [19]. By constraint in the specification of SystemC-AMS described above, one time step delay on the computation occurs between the ELN MoC and the TDF MoC. In the cases of [6] and [9] that is depicted in Fig. 4. 1 (a), the non-linear I-V characteristic is directly expressed as a voltage-controlled current source on the TDF MoC. In these cases, the voltage on the MOSFET is calculated on the ELN MoC at a time step, and is converted into the TDF MoC by using the predefined ELN module

sca_eln::sca_tdf_vsink. Then, based on the value of the voltage, the current is calculated and updated on the TDF MoC. The updated current is reflected into the value of the current on the ELN MoC through the predefined ELN module sca_eln::sca_tdf_isource after one time step delay (at next time step). In other words, the consistency between the voltage and the current on the ELN MoC is not maintained in each time step. Particularly, in the case of circuit simulation for such as an UIS test circuit with steep switching, it causes non-convergence or has a inaccurate effect on results of the simulation of SystemC-AMS.

In our technique that is depicted in Fig. 4. 1 (b), we model the power MOSFET as an on/off switching resistance, which is a voltage-controlled resistor on the TDF MoC. And it is connected into the ELN MoC with using the predefined ELN modules such as sca_eln::sca_tdf_r. It enables the consistency between the voltage and the current on the ELN MoC to be maintained in each time step. In other words, on the MOSFET, Ohm's law is always held. However the value of the on/off switching resistance is updated with one time step delay because of the above mentioned same reason. We are able to suppress the influence of the delay as much as possible with setting a time step interval small. Furthermore, with above mentioned similar technique, we model a diode as a resistance (equivalent diode model) that the current flows only to a one direction, and apply its model to such as a body diode and a avalanche breakdown diode.

The on/off switching resistance is the most important characteristic in the MOSFET. Since the value of the drain-source voltage (V_{ds}) is very small (less than a few hundred mV) in the on-state (on-region) of the MOSFET, we derived a simple characteristic equation of the on/off switching resistance by simplifying the equation of SPICE LEVEL 1 [3], [5]. Figure 4. 2 depicts the simple characteristic equation. Then, based on the characteristics of the threshold voltage and on-resistance shown in [10]-[11] and [16], we set the values of threshold voltage (V_{th}) and channel conductance (β), and calculated their temperature coefficients (TCV_{th} and $TC\beta$).

Figure 4. 3 depicts our SystemC-AMS electrical power MOSFET model. The model is mainly composed of a on/off switching resistance (R_{ds}), an effective avalanche breakdown voltage ($BV_{dss(eff)}$), two equivalent diode models of the body diode and avalanche breakdown diode, and a body resistance (R_{body}). In addition, a drain-source capacitance (C_{ds}), a gate-source capacitance (C_{gs}), and a gate-drain capacitance (C_{gd}) are added, which are calculated based on capacitance parameters of [10]-[11] and [16]. Thus our model is very simple. We show the values of main model parameters and temperature coefficients at room temperature (T_{nom}=298.15 [K]): β_0=40.0 [A/V2], V_{th0}=2.8 [V], C_{ds}=2.65e-9 [F], C_{gs}=4.40e-9 [F], C_{gd}=1.70e-9 [F], $R_{ds(on)}$=3.5e-3 [Ohm], $R_{ds(off)}$=1.0e12 [Ohm], R_{body}=1.0e15 [Ohm], BV_{dss}=53.3 [V], $BV_{dss(eff)}$=1.3×BV_{dss}=69.3 [V], TCV_{th}=-3.57 [1/K], and $TC\beta$=-2.1 [-]. Furthermore, with respect to the temperature coefficients of the avalanche breakdown voltage, and those of the equivalent diode models of a body diode and an avalanche breakdown diode, we used the values that are shown in [10]-[11] and [16]. In our electro-thermal simulation with SystemC-AMS, we combine our SystemC-AMS electrical power MOSFET model and the thermal equivalent circuit model shown in Fig. 3. 2. We call it SystemC-AMS electro-thermal model (our SystemC-AMS model).

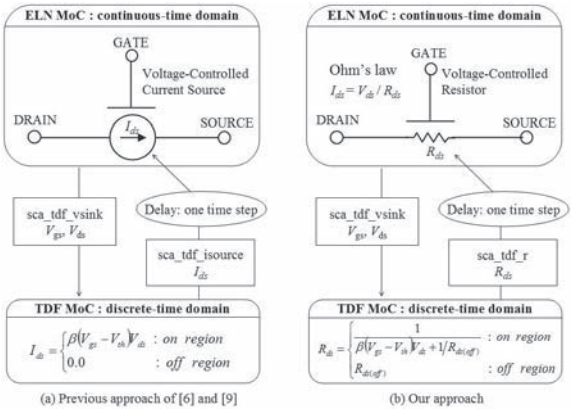


Fig. 4.1: our implementation method for the I-V characteristic of a power MOSFET with TDF MoC.

$$V_{th} = V_{th0}\left[1.0 + TCV_{th}\left(V(T_h) - T_{nom}\right)\right]$$

$$\beta = \beta_0\left(\frac{V(T_h)}{T_{nom}}\right)^{TC\beta}$$

$$R_{ds(on)} = \frac{1.0}{\beta\left(V_{gs} - V_{th}\right) + \dfrac{1.0}{R_{ds(off)}}}$$

$$R_{ds} = \begin{cases} R_{ds(on)} : V_{gs} > V_{th} & (on-reigon) \\ R_{ds(off)} : V_{gs} <= V_{th} & (off-reigon) \end{cases}$$

Fig. 4.2: our simple characteristic equation for the on resistance of a power MOSFET.

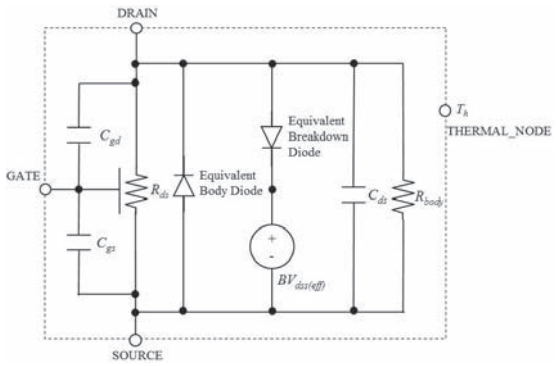


Fig. 4.3: our SystemC-AMS electrical power MOSFET model .

Next we consider a numerical integration method that is implemented in the DAE solver of SystemC-AMS. As described in the Section II, The UIS test is a steep switching circuit, and hence it causes sudden transient changes of the signals on time domain. In our experimentation, due to the sudden transient changes of the signals, SystemC-AMS with

classical backward Euler method and trapezoidal method induced numerical oscillations[2]. The same problem related to numerical instability issues is also reported in the study of [8]. The work of [8] uses fourth-order Runge-Kutta method to improve it.

In contrast, we use a new method so-called Adams-Moulton method [13], which is with the accuracy that is equal to fourth-order Runge-Kutta method, and is more efficient. As a result, we were able to improve the problem greatly.

V. Experimental Results

As our experimental verification, we applied the above mentioned technique to electro-thermal circuit simulation of the UIS test circuit of [10]-[11] that is depicted in Fig. 5. 1. The circuit is composed of an electronic circuit and a thermal circuit. Note that the thermal circuit include a thermal resistance (R_{thp}) and a thermal capacitance (C_{thp}) that expresses thermal conduction from package case to ambient. We considered simulations of the following three cases. (1) PSPICE simulation with using the model of [10]-[11] which is a subcircuit of PSPICE. (2) SystemC-AMS simulation with using our power MOSFET model. (3) NGSPICE simulation with using our power MOSFET model. The reason that set case (3) is to use it as another reference. In the case of (3), we implemented our power MOSFET model into NGSPICE [17] with using XSPICE [21]. XSPICE is a C based modeling tool that has been developed by the Georgia Institute of Technology. We ran these simulations on HP dv9700 (OS Vista, CPU Intel Core2 Duo 2.5GHz, RAM 4.00 GB). Figure 5. 2 depicts the simulation results of case (1), case (2), and case (3) [3]. Table I shows the CPU time for each of the three cases.

The simulation results for each of case (2) and case (3) almost correspond with those of case (1), and hence the results demonstrate the adequacy of our technique for electro-thermal modeling and simulation. In the case of (2), it is necessary that the simulation time step interval is set small in order to simulate steep switching behaviours of the UIS test circuit. In this case, we set 1.0e-9 second as the value of the time step interval. Therefore, the simulation run-time increases. The simulation run-time of case (1) is about four times longer than that of case (3). The reason is due to the complexity of the model of [10]-[11] used in the case (1), and the difference in circuit simulators.

Furthermore, Fig 5. 3 depicts the SystemC-AMS simulation results of the case that the device junction temperature is not fed back from the thermal circuit to the electronic circuit. The drain-source avalanche breakdown phenomenon is underestimated in comparison with the simulation results shown in Fig. 5. 2. The almost same results as shown in Fig 5. 3 were also obtained by PSPICE simulation using the model of [10]-[11].

[2]It was not able to be solved even by using ultra small time step.
[3]Note that the device junction temperature is expressed by unit of deg. C in the Fig. 5.2 and Fig. 5. 3.

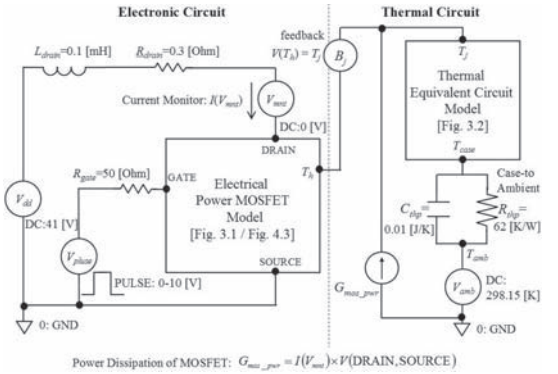
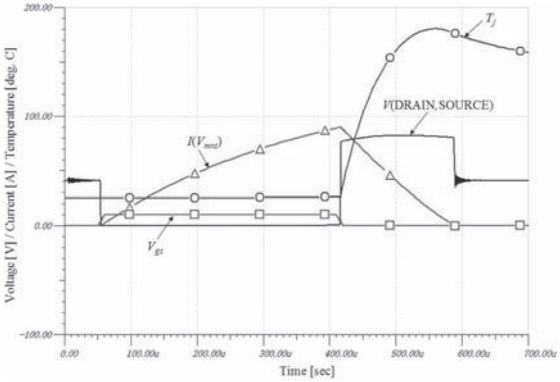
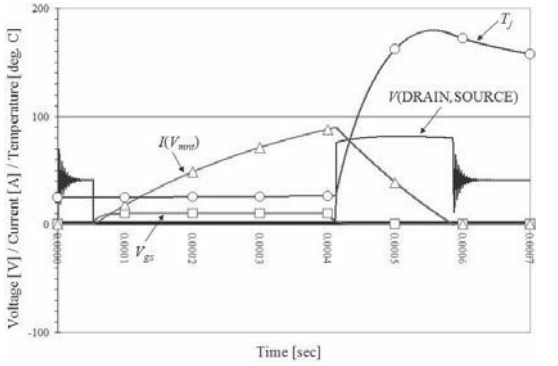


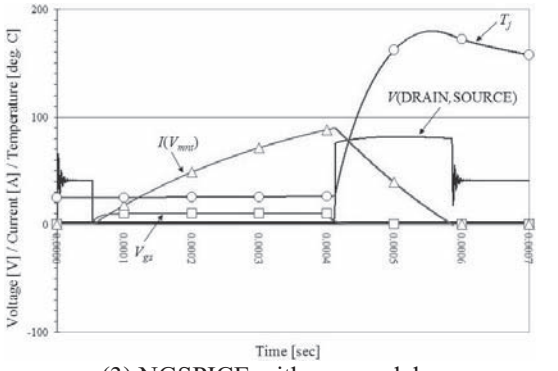
Fig. 5.1: Schematic for the electro-thermal simulations of an UIS test circuit.



(1) PSPICE with using the model of [10]-[11]



(2) SystemC-AMS with using our model



(3) NGSPICE with our model

Fig. 5.2: Simulation results of UIS test circuit.

(1) PSPICE	(2) SystemC-AMS	(3) NGSPICE
50.5 [sec]	139.2 [sec]	12.2 [sec]

Table I: Processing CPU times of the simulations.

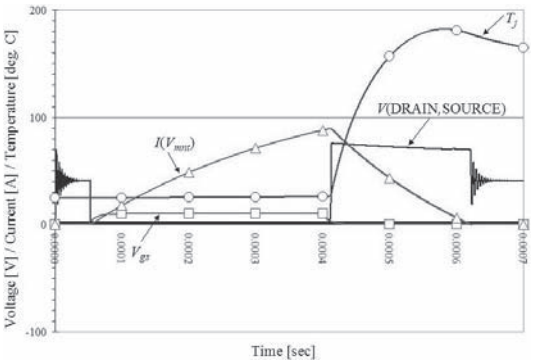


Fig. 5.3: Our SystemC-AMS simulation result of the case of non-feedback from thermal circuit to electronic circuit.

VI. Conclusions

We have proposed a new technique for the electro-thermal modeling and reliability simulation with SystemC-AMS. It starts with the modeling of non-linear devices such as a power MOSFET and a diode by using TDF MoC. It then implements a new numerical integration method so-called Adams-Moulton method to solve numerical instability issues of SystemC-AMS. Furthermore, we applied our technique to electro-thermal and reliability circuit simulation of an UIS test circuit. Our technique was demonstrated by experimental results.

In our experiments, we needed to set simulation time step interval small so that a steep switching circuit is able to be handled by SystemC-AMS. As a result, its simulation run-time increased. We are improving the LU decomposition solver of SystemC-AMS in order to reduce the run-time.

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