A Third Order Delta-Sigma Modulator with Shared Opamp Technique for Wireless Applications

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Abstract — this paper described the design of A third orders delta-sigma modulator (*DSM*) exploited shared opamp technique in order to reduce number of opamp required, consequently the total power consumption for the modulator decreased as well as required area decreased too. The architecture relaxed comparator speed which appropriate for wireless applications. First and second stages are sharing one opamp in integration and sampling phase. The proposed circuit has been designed on *TSMC* 0.18um *CMOS* technology. 2*MHz* Bandwidth, 50dB Peak *Signal-to-Quantization-Noise Ratio (SQNR)*, which is suitable for *WCDMA*, have been achieved. It consumes 2.4mW with power supply 1.2V and area is 0.3mm^2.

I. INTRODUCTION

High order loop filter is one of conventional approach to attain high resolution delta-sigma modulator (*DSM*) which required an opamp for each integrator. The conventional third order 1-bit *DSM* required three amplifiers. However, amplifier is used only in one phase of clock period for signal integration. In order to use two phases of clock period for signal integration without increasing in the supply current of amplifier, there are two approaches one is "double sampling "switch capacitor (*SC*) integrator which increase over sampling ratio(OSR) and other is time sharing technique which increase DSM order. The advantages of time sharing technique are decreasing number of opamp required for the same order, low power consumption, no mismatching in sampling capacitor like double sampling technique [1] and low area. Time sharing amplifier technique has been previously published in *SC* filters, *DSM* for audio applications [2]. A *DSM* for audio applications has been employed a third order *DSM* using one opamp [3], it requires a very high speed quantizer which is very difficult to implement in wireless applications. In order to relax the quantizer speed, one more opamp has been adding for third integrator. Moreover, feed-forward technique has been applied to relax the performance of analog component [4].

This design targets to *WCDMA* applications that required the highest bandwidth1.92MHz and over 50dB *SQNR*. In this paper a proposed third order, feed-forward, and 1-bit quantizer *DSM* with two opamp is presented. Shared-amplifier technique for first and second integrator has been provided. The proposed circuit has been simulated using *TSMC* 0.18um process.

II. PROPOSED CIRCUIT AND DESIGN SIMULATION

Fig. 1 illustrates fully-differential circuit schematic of the proposed *DSM*. The circuit is composed of two opamps, an analog adder and 1-bit quantizer. The first opamp is used to realize first and second integrator. It is required $T_s/2$ to perform integration for each stage. $C_{s1}$and C_{s2} are a sampling capacitor for the first and second integrator respectively, in addition, C_{i1} and C_{i2} are integration capacitor for first and second integrator correspondingly.

The second opamp realized third integrator using C_{s3} and C_{i3} for sampling and integration phase respectively which required half cycle for each phase, therefore the comparator has adequate time to make decision. C_{a1}, C_{a2}, C_{a3} and C_{a4} have been used to implement a passive analog adder for 1-bit quantizer. Q_1 and Q_2 are non-overlapped clock, Q_{1d} and Q_{2d} are delayed clock for Q_1 and Q_2 respectively . Fig. 2 show the timing diagram for each stage of the proposed circuit. When Q_2 is high, the input signal is sampling by C_{s1}, during the sampling phase for the first stage, the first opamp is busy in integration for the second stage. The capacitor charge of C_{s2} transferred to C_{i2} then sampled by C_{s3}. When Q_1 is high, the capacitor charge of the C_{s1} transferred to C_{i1} then sampled by C_{s2}. The passive adder summed the charges when Q_1 is high except the charges come from second stage that inverted and transferred to C_{a3} when Q_2 is high. The output of the passive adder was quantized by the comparator when Q1 is high.

The proposed *DSM* circuit is designed on *TSMC* 0.18µm technology with 1.2V supply. The circuit has been design in fully differential. Sampling clock (F_s= 80MHz) has been used to generate non-overlapped clock (Q_1, Q_2). Bandwidth and DC gain for the opamp were designed to be 250MHz and 45dB respectively and power consumption is 1.1mW that meet the requirements of *WCDMA* specifications. The output spectrum of circuit simulation with -6dBFS sine-wave with 500KHz input frequency has been illustrated in Fig.3. Table 1 shows the result summary of proposed circuit compared to other result using [5]. Where P is power consumption, *N* is the effective number of bits F_B is the signal bandwidth The Figure of Merit (FoM) of the modulator was written as following:

$$FoM = \frac{P}{2^N \cdot 2 \cdot F_B} \quad (1)$$

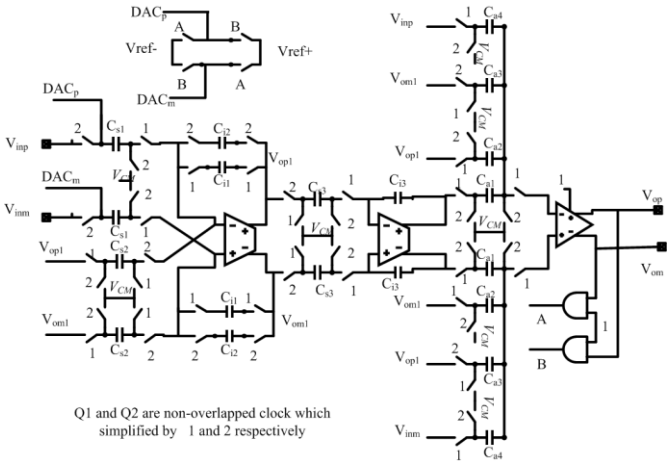

Fig.1 proposed circuits for 3rd order DSM Modulator.

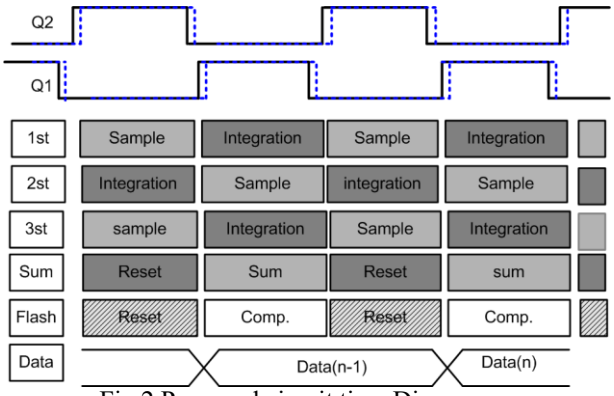

Fig.2 Proposed circuit time Diagram

Table I Performance summary

Parameter	[5] 2009(ISSCC)	This work
Power Supply	1.2v	1.2v
Technology	0.18µm	0.18µm
Sampling frequency	80MHz	80MHz
Bandwidth	2MHz	2MHz
SQNR	58dB	50dB
Power consumption	6.43mW	2.4mW
FoM(P/fs[pJ])	2.47	2.32

Table1. Shows the design parameter and result of the proposed design that attains a FoM of 2.32pJ/Conv.Step.which is lesser than [5] the modulator achieves a lower figure of merit. Fig.4 shows the circuit's simulation power spectrum density.Fig.5 shows layout of the proposed circuit and clock generator which is 0.3mm2.

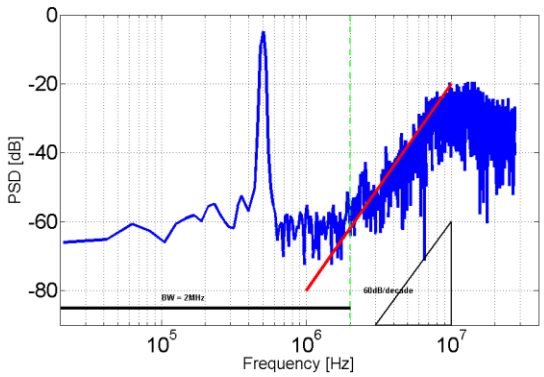

Fig.3 Output spectrum of spectre circuit simulation.

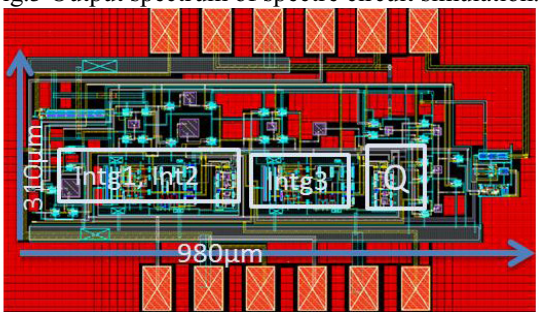

Fig.4 Proposed circuit layout.

III. CONCLUSION

Shared amplifier technique has been applied in a third order *DSM* to decrease number of amplifiers required. Moreover, decrease the power consumption. The proposed DSM has been designed and simulated employing *OSR=20*. The proposed DSM has achieved *SQNR 50dB* for *-6 dBFS*, 2.4 mW power dissipation, and *2MHz* bandwidth.

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