

# A Design of 2GHz Band O-QPSK Wireless Transmitter using 0.18 $\mu$ m CMOS Technology

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**Abstract**—Brain-Machine-Interface(BMI) has been attracted attention in recent years, and the demands for wireless communication are increasing. In this paper, we proposed a transmitter using O-QPSK on 0.18 $\mu$ m CMOS technology to meet the requirements for wireless communication. This transmitter operates at 1V supply voltage, and current consumption is 15.03mA. Output is -3dBm, and the maximum data rate is 12.8Mbps.

## I. INTRODUCTION

BMI which conducts bidirectional communication between Brain and Machine has been attracted in attention in recent years. For example, this system has been expected to realize bionic hand and bionic leg about in medical field. In order to develop BMI, we have developed a system which is available to sense neural signals and stimulate neural cells using Micro-Electrode-Array(MEA) and Large-scale-integration(LSI)[1]. On the other hand, progressing study of BMI ,demands for wireless communication are increasing. Currently, all experiments are in wired from neural cells to PC. However this composition limits the flexibility of the experiment, because of cable length. Also, wireless is very important to avoid the burden of human activities realizing BMI. To solve this problem, we tried to realize wireless communication (Fig.1(a)). In this study, sending the neural signals which caught at current neural recording system to computer in wireless using 0.18 $\mu$ m CMOS technology. In the transmission, this system adopted offset QPSK(O-QPSK) which relaxes requirements of Power Amplifier's (PA) linearity. For typical value, the sampling rate is 20kS/s, 10-bit, channels are 16-64, respectively. The data rate can calculate as Data rate = sampling rate  $\times$  bits  $\times$  channels. Thus, the required data rate is 3.2Mbps-12.8Mbps. This paper is organized as follows. Section II, the transmitter architecture is introduced. In section III, the simulation results are shown. Finally, Section IV is conclusion.

## II. SYSTEM ARCHITECTURES & MODULE DESIGN

To reduce the area of chip and the current consumption, we consulted the previous study for a sys-

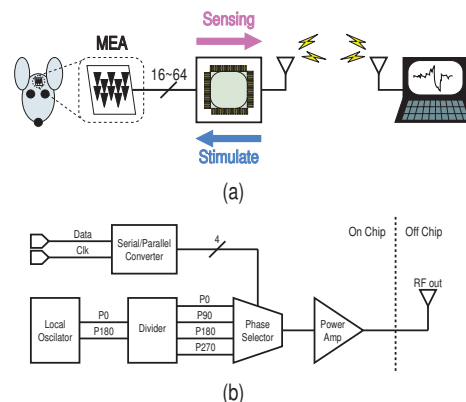


Fig. 1. (a)BMI system's consist of wireless.(b)System architecture of transmitter.

tem architecture (Fig.1(b))[2]. It consists of Serial / Parallel Converter(S/P Converter), Voltage Controlled Oscillator(VCO), Divider, Phase Selector(PS) and Power Amplifier(PA). For Phase Selector, we referred previous circuit[2]. In order to reduce the power consumption, all of circuit are supplied by 1V supply Voltage. S/P Converter produces O-QPSK signals I,Q. When signals I,Q change at the same time(ex.[I,Q]:[0,0] $\rightarrow$ [1,1]), S/P Converter made half clock delay before changing Q. For the local oscillator, conventional N-type voltage-controlled oscillator(VCO) has been chosen. VCO connected to the source follower(SF) as a buffer. The schematic of the VCO and SF are shown in Fig.2. In order to operate at high Q-factor, this VCO oscillates at 4GHz band. The VCO outputs P0 and P180 have 180 $^{\circ}$  phase difference. Previous studies have proposed a number of dividers. With them, in this time, we choose a conventional circuit as a reference (Fig.3)[3]. This architecture can reduce required power supply and current consumption. Previous stage outputs  $\Phi$  and  $\bar{\Phi}$  input to the CLK and  $\overline{\text{CLK}}$ , and the carrier frequency is divided by two. Moreover, divider's output P0 ~ P270 which were shifted by 90 $^{\circ}$  phase. Unlike a conventional transmitter, this architecture is composed without using a

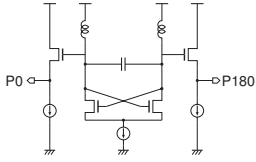


Fig. 2. VCO and SF.

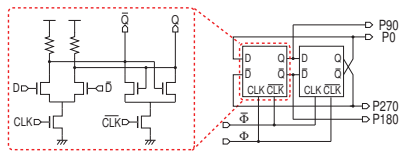


Fig. 3. Divider.

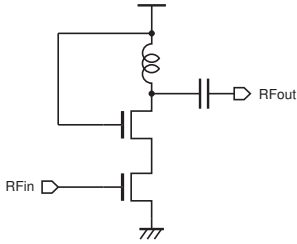


Fig. 4. Cascode type PA.

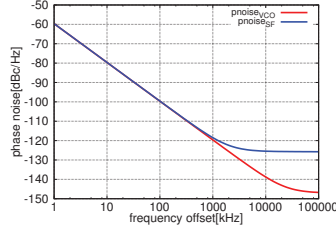


Fig. 5. Phase noise of VCO and SF

mixer. Phase selector just takes the configuration of the MOS, so the area of chip and the power consumption can be reduced. For PA, we chose cascode type PA(Fig.4)[4]. Output impedance of this PA matched at  $50\Omega$ .

### III. SIMULATION RESULTS AND LAYOUT

Phase noise of VCO and SF are shown in Fig.5. As an indication of VCO's figure of merit, there are two values called power frequency normalized(PFN), power frequency tuning-normalized(PFTN).

$$PFN = 10 \cdot \log \left[ \left( \frac{kT}{P_{DC}} \right) \cdot \left( \frac{f_{OSC}}{f_{offset}} \right)^2 \right] - L\{f_{offset}\} \quad (1)$$

$$PFTN = 10 \cdot \log \left[ \left( \frac{kT}{P_{DC}} \right) \cdot \left( \frac{f_{TUNE}}{f_{offset}} \right)^2 \right] - L\{f_{offset}\} \quad (2)$$

$P_{DC}$  is the power consumption,  $f_{OSC}$  is oscillating frequency,  $f_{TUNE}$  is variable frequency,  $f_{offset}$  is offset frequency and  $L\{f_{offset}\}$  is phase noise at a offset frequency( $f_{offset}$ ). The calculated PFN and PFTN are 22.14dB and -3.87dB at  $f_{OSC}=4\text{GHz}$ ,  $f_{offset}=1\text{MHz}$ . Fig.6 shows the simulation results of PA. According to this figure, the maximum power added efficiency(PAE) is 22% when input is 2dBm. While the output is saturated from -5dB the input, linearity of the PA request has been relaxed because of adopting O-QPSK as a wireless system. Fig.7 shows the PA output waveform correspond to the the signal change of [0,0] to [1,0] at the data rate 12.8Mbps, it can see the phase changing. We confirmed the simulation results in each modules. This transmitter consumes 15.03mA and outputs -3dBm. Fig.8 shows a chip layout and Fig.9 shows a chip photograph. The proposed transmitter is fabricated in a standard  $0.18\mu\text{m}$

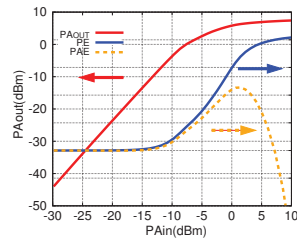


Fig. 6. Simulation result of PA.(output power,PE and PAE)

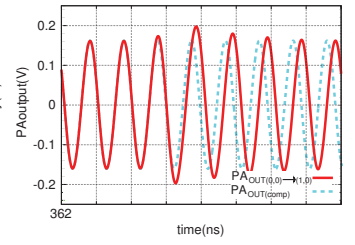


Fig. 7. Comparison of the PA's output waveform.

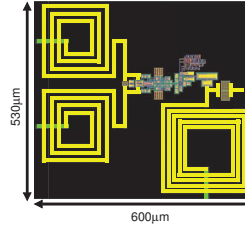


Fig. 8. Chip layout.

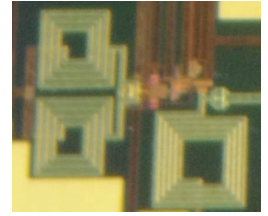


Fig. 9. Chip photograph.

CMOS technology. The size of the core area is about  $530\mu\text{m} \times 600\mu\text{m}$ .

### IV. CONCLUSION

In this study, 2GHz Band O-QPSK Wireless Transmitter using  $0.18\mu\text{m}$  CMOS technology has been demonstrated. This transmitter operates at 1V supply voltage and current consumption is 15.3mA. Combining with existing systems, it will offer great advantages for the future of BMI's applications.

### ACKNOWLEDGEMENTS

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