Highlights

Keynote Speeches

K1 Keynote Speech I

Thursday, March 8, 2012, 9:15 - 10:15 [Int'l Conf. Room]

Robust System Design: Overcoming Complexity and Reliability Challenges

Subhasish Mitra

Stanford University, USA

Abstract

Today's mainstream electronic systems typically assume that transistors and interconnects operate correctly over their useful lifetime. With enormous complexity and significantly increased vulnerability to failures compared to the past, future system designs cannot rely on such assumptions. At the same time, there is explosive growth in our dependency on such systems. Robust system design is essential to ensure that future systems perform correctly despite rising complexity and increasing disturbances. This talk will address the following major robust system design goals: 1. New approaches to thorough test and validation that scale with tremendous growth in complexity; and, 2. Cost-effective tolerance and prediction of failures in hardware during system operation. Significant recent progress in robust system design impacts almost every aspect of future systems, from ultra-large-scale networked systems, all the way to their nanoscale components.

K2 Keynote Speech II

Friday, March 9, 2012, 9:00 - 10:00 [Int'l Conf. Room]

Parallelization, Customization and Automation

Jason Cong

University of California, Los Angeles, USA

Abstract

In order to meet ever-increasing computing needs and overcome power density limitations, the computing industry has halted simple processor frequency scaling and entered the era of parallelization, with tens to hundreds of computing cores integrated in a single processor, and hundreds to thousands of computing servers connected in a warehouse-scale data center. However, such highly parallel, general-purpose computing systems still face serious challenges in terms of performance, power, heat dissipation, space, and cost. We believe that we need to look beyond parallelization and focus on domain-specific customization to provide capability of adapting architecture to application in order to achieve significant power-performance efficiency improvement. This paradigm shift requires a great deal of innovation in architecture, compilation, and runtime system design, and offers many exciting and challenging research opportunities. I shall discuss the research progress in this direction and implication to the EDA industry.

Invited Talks

I1 Invited Talk I

Thursday, March 8, 2012, 13:30 - 14:30 [Int'l Conf. Room]

Energy Harvesting for Self Powered Sensor Systems – Case Study: Vibration Energy Harvesting for 'Intelligent Tire' Application –

*Rob van Schaijk, Rene Elfrink, Valer Pop, and Ruud Vullers

Imec / Holst Centre, The Netherlands

Abstract

Wireless autonomous sensor systems become steadily standard components in our environment and they become smaller, cheaper and more sophisticated. System autonomy during its intended lifetime is not reached in case batteries are used due to size limitations and the need to recharge. Aim is to generate and store power at the micro-scale to improve autonomy and reduce size. Energy harvesters fabricated by micro-system technology can realize this goal. The choice of harvesting principle depends on the application and vibration, thermal, photovoltaic and radiofrequency power conversions are investigated at imec/Holst Centre. An overview of latest results and remaining challenges will be given with the focus on vibration energy harvester. Vibration energy harvesters are of specific interest for machine environments where sinusoidal vibrations or repetitive shocks are present. In this presentation the application focus will be on tire pressure monitoring systems (TPMS) and 'intelligent tire' applications. Measuring pressure and in the future more vital parameters, like e.g. forces, will improve safety and reduce fuel consumption. Vibration energy harvesters can provide sufficient power to accommodate autonomy in these applications. The design and characterization of piezo-electric energy harvesters will be presented together with dedicated power management solutions. Also the 'intelligent tire' concept will be introduced and system optimization of fully autonomous wireless sensor systems mounted in the tire will be discussed.

I2 Invited Talk II

Friday, March 9, 2012, 13:15 - 14:15 [Int'l Conf. Room]

Innovating the SoC Design for Emerging Memory Technologies

Sungjoo Yoo

POSTECH, Korea

Abstract

A new emerging memory technology, Phase-change RAM is gaining more and more attention as a complement or replacement of existing DRAM in the main memory subsystem. In order for PRAM to be applied to the main memory, its limitations of write endurance, long read/write latency, high write power consumption need to be overcome on the PRAM chip and the SoC utilizing the PRAM. In this paper, we explain recent works on innovating SoC designs to better utilize PRAM-based main memory.

I3 Invited Talk III

Friday, March 9, 2012, 16:00 - 17:00 [Int'l Conf. Room]

K Computer: Challenges making the Superior Quality Interconnect

Takahide Yoshikawa

Fujitsu Laboratories, Japan

Abstract

The K computer, RIKEN and Fujitsu are now developing, has twice been awarded the title of the world's fastest computer by the TOP500 project. Throughout development, lots of bugs were detected, but these bugs were fixed before manufacturing. This was achieved by our advanced verification methodologies. Furthermore, the 88,128 nodes system can run 30 hours without any single fault. This was supported by our leading production test methodologies. This paper introduces these advanced verification and production methodologies.

Panel Discussion

D Panel Discussion

Thursday, March 8, 2012, 16:30 - 18:00 [Int'l Conf. Room]

Challenges for Future System Design and Verification

Organizer: Shinji Kimura (Waseda University, Japan)

Panelist: Jason Cong (University of California, Los Angeles, USA)
Subhasish Mitra (Stanford University, USA)
Rob van Schaijk (Imec / Holst Centre, The Netherlands)
Sungjoo Yoo (POSTECH, Korea)
Takahide Yoshikawa (Fujitsu Laboratories, Japan)

Abstract

Process shrinking does not stop, and tons of transistors can be integrated in one chip. We also have 3D-IC for integrating a memory chip on a CPU chip or so, and novel non-volatile memory technologies seem to be available in the near future. We can use such huge and various resources to implement highly parallel information systems. However the design, synthesis, and verification become complicated because of the system complexity, the unreliable behavior of devices such as the process variation, single event upset, etc.

Power issue is also very important in system design. After 311 earthquake and the related nuclear plant problem in Japan, energy supply has been paid attention from the point of view of the sustainable life, and power consumption of information systems are discussed seriously since information systems become the basis of social activities and such systems cannot be stopped.

Based on those observations, we would like to discuss about the problems and solutions on future system design and verification in the panel. 5 panelists gathered from various areas will clarify images of promising future systems, problems and prospective solutions on electronic design automation of parallel systems, reliability issues, power harvesting issues, memory issues, and massively parallel system issues, etc.