Ultra Low Current Measurement with On-chip High Resistance of MOSFET Array

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Abstract— We propose on-chip high resistance using MOSFET array. We adopt the potentiostat method as an electrochemical sensing to measure ultra low current being aware of biosensing and implant sensing. The sensor circuit includes a high resistance array which is configured by connecting unit resistors in series and parallel. We verify the DC characteristics, the area, and the temperature characteristics of the resistor array by the SPICE simulation, then demonstrate the promising result compared with the conventional Poly resistance.

I. Introduction

As advancing in biosensing technology and implant sensing technology, the diversification of the sensor front end has progressed and the demand for high performance against ultra low current measurement has been increasing. Many current measurement circuits in the past are high-performance, large-sized.In particular, in order to miniaturize the circuit, a method of realizing on-chip high resistance is required. We focus on the current measurement circuit used in the potentiostat among the electrochemical measurement methods and propose a current measurement circuit capable of detecting ultra low currents less than 1nA while realizing a small area by realizing high resistance by MOSFET array.

For a high resistance implemented in an LSI, it is common to use polysilicon with a sheet resistance as high as the number of $k\Omega/sq.$. However, for example, if a high resistance of 1GΩ or more even with the sheet resistance is high, it takes a large area. The current measurement circuit used in this work consists of a basic current-voltage conversion circuit (I-V conversion circuit), which converts a current into voltage by the resistance. When obtaining an output of 1V from a 1nA current, we need 1GΩ of resistance, so it is not suitable for one-chip of circuit to deal with a weak current.

Therefore, in this work, we propose a method to construct a high resistance of 1GΩ or more with a small area by operating the MOSFET in the subthreshold region. The subthreshold region is an operating region of the MOSFET where the gate voltage of the transistor is lower than the threshold voltage, but in this case, high resistance is obtained by operating with the gate completely off. Since the source voltage is always grounded by using the virtual ground of the operational amplifier used for the I-V conversion circuit, this makes it possible to operate the transistor while the gate is always off.

The rest of this paper is organized as follow. Section II introduces a mechanism of the potentiostat and I-V conversion. Section III describes the configuration of our on-chip resistance. Then, section IV demonstrates the result of comparing Poly resistance and recommends configuration of resistance arrays based on SPICE simulation results. Section V concludes this work.

II. Potentiostat Method

The potentiostat method is one of methods for quantitative and qualitative analysis of ions and residual substances in electrochemical measurements. It applies an electric signal to a cell and generating a chemical reaction, and a chemical reaction occurring internally is analyzed from the response signal. Measurements are divided into two methods. one measures the potential difference and the other does the current, and the potentiostat is the latter.

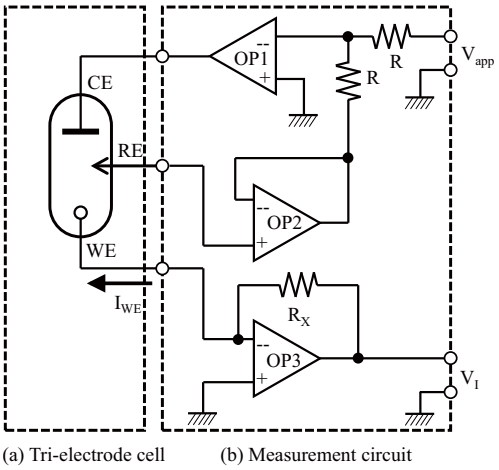

Fig. 1. Potentiostat method

A. Tri-electrode Method

In this paper, the proposed on-chip resistor is assumed to be applied to a potentiostat for tri-electrode-type electrolytic cell, so we explain tri-electrodes used for potentiostat.

A typical electrochemical measurement method has a working electrode (WE), a counter electrode (CE), and a reference electrode (RE) as shown in Fig. 1 (a), and it is called a tri-electrode method. 'WE' is an electrode for detecting an object to be measured, 'CE' is an electrode for applying and regulating a voltage between the other two electrodes, 'RE' is an electrode for taking a reference potential.

A simple operation of tri-electrode method is as follows.

1. The potentiostat makes the potential of 'WE' constant with respect to that of 'RE'
2. 'WE' electrolyzes the target sample on the electrode.

3. The current required to maintain electrolysis at 'WE' flows from 'CE'.

4. At this time, the potentiostat accurately measures the current flowing from 'WE' and 'CE'. Notice that no current flows through 'RE'.

B. Potentiostat Operation

We describe the operation principle of the potentiostat and the basic circuit configuration with operational amplifiers (op-amps). Potentiostat for tri-electrode cell controls a voltage between T_{WE} and T_{CE}, shown in Fig. 1 (a), such that the potential (E_{WE}) of T_{WE} against the potential (E_{RE}) of T_{RE} becomes to be equal to the externally applied voltage (V_{app}). That is; $V_{app} = E_{WE} - E_{RE}$. Assuming that T_{WE} is grounded, that is $E_{WE} = 0$, $V_{app} = -E_{RE}$. A circuit satisfying these equations can be configured for an inverting amplifier.

Although some components might be added for the stable operation, the basic circuit of the potentiostat is constituted by the circuit shown in Fig. 1 (b). In Fig. 1 (b), it outputs a voltage to satisfy the above two equations since OP1 is virtually grounded at IN-. Regardless of 'RE' potential difference for 'CE' ($E_{RE} - E_{CE}$), the circuit outputs $-V_{app} + (E_{RE} - E_{CE})$. OP1 conducts the same current as flowing between $T_{CE} - T_{WE}$ in the tri-electrode cell. Also, in actual experiments, it is necessary to use a voltage follower (OP2) so that the operation of the circuit is not affected even if a current flows through the reference electrode 'RE'. As a result, we can measure the current I_{WE} flowing between 'WE' and 'CE'. Plus, we convert the obtained current I_{WE} into voltage by I-V conversion circuit (OP3) for digital processing of sensing value. Hence, since I_{WE} is from 'WE' to 'CE', the output of the potentiostat is as; $V_I = I_{WE} \cdot R_x$.

In this paper, we use MOSFET to convert resistance R_x of the I-V conversion circuit of Fig. 1 (b) to operate as a resistor.

All op-amps used in this work has the following specifications; the DC gain = 84.735 dB, the cut-off frequency = 2.567 kHz, the unity · gain frequency = 42.635 MHz, the phase margin = 74.921 deg., the input voltage range = 0.752 V to 4.713 V, the output voltage range = 0.146 V to 4.894 V, the offset voltage = 0.108 V.

III. Our On-chip Resistance Configuration

We propose a resistor utilizing the characteristics in the subthreshold region of MOSFET. In this section, we illustrate the configuration of the resistance that can be used as the equivalent resistance R_x of the I-V conversion circuit in the potentiostat in the previous section. Assuming a ultra low current of several nA to several tens of fA, we configure resistors with six resistance values, 1 GΩ, 10 GΩ, 100 GΩ, 1 TΩ, 10 TΩ, 100 TΩ. In the circuit, each resistance value is realized by series and parallel connections of unit resistors.

A. Configuration and Unit Resistance

First, we consider the resistance value of the MOSFET in the subthreshold region. The drain current in the subthreshold region is;

$$I_{ds} = I_0 \exp\left(\frac{V_{gs} - V_{th}}{nV_t}\right) \cdot \left(1 - \exp\left(-\frac{V_{ds}}{V_t}\right)\right) \quad (1)$$

$$I_0 = \mu C_{ox} \frac{W}{L}(n-1)V_t^2, \quad (2)$$

where μ is the mobility, C_{ox} is gate oxide capacitance, n is a parameter of the subthreshold, L is channel length, W is channel width, and V_t is thermal voltage. In $V_{DS} > 0.1V$, especially, I_{ds} is approximated as;

$$I_{ds} = I_0 \exp\left(\frac{V_{gs} - V_{th}}{nV_t}\right). \quad (3)$$

In this work, the MOSFET is assumed to be operated with the gate completely off. Actually, the current flowing through the MOSFET is not completely cut off, and a little current flows between the drain and the source. This current is called gate-off leak current I_{ds0}. The gate-off leak current is generally thought to have a correlation with the threshold voltage, but it can not be theoretically derived. Therefore, it is necessary to obtain this current value from simulation according to the process model to be used.

In this paper, we verify the I-V characteristic in the subthreshold region in the 0.6 μm process model dealt with. Notice that a finer process is not always appropriate as long as gate-off peak current is employed. The results of the SPICE simulation are shown below.

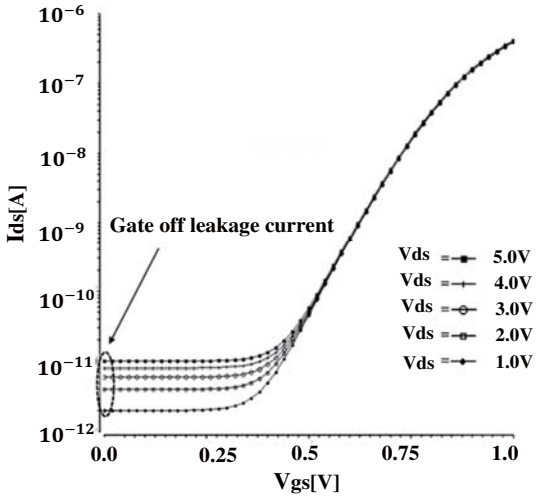

Fig. 2. I-V characteristics of MOSFET

The simulation results confirm us that the resistance value of about 500 GΩ can be obtained when the gate-off leak current flows through the MOSFET under the condition of $V_{gs} = 0$.

B. Appropriate Transistor Size

When operating at $V_{gs} = 0$ for the MOSFET, the transistor size affects its resistance value. We select an appropriate tran-

sistor size by clarifying the relationship between transistor size and the resistance value.

By simulation, we observe the resistance decreases greatly when the channel length L becomes smaller than 5 μm. The detailed data is omitted for the space. This change in the resistance value is thought to be due to the channel length modulation effect. As discussed above, the accuracy of resistance device approaches 500 GΩ as resistance accuracy increases. As a result, a larger channel length L and a smaller channel width W of the MOSFET tends to give a higher accuracy.

Plus, in this paper, we attempt to configure a larger resistor by connecting many resistors of the same size (i.e. unit resistor) in parallel and in series. The unit resistor is realized by a unit transistor, and its channel size is desired to be smaller for the one-chip implementation. Considering both the accuracy and the area, in this paper, the size of MOSFET is channel length L = 6.4 μm and channel width W = 1.6 μ m.

C. Resistance Configuration

Since the value of the gate-off resistance per a unit transistor is about 500 GΩ, the desired resistance value is obtained by changing the number of connections in series and in parallel. This resistor is used as the resistor of the I-V conversion circuit of the potentiostat. We try to configure the resistor such that the resistance value changes by 1 digit each time of the measurement current changing by 1 digit in the range from 1 nA to 10 fA. It is realized by changing the number of connections of 500 GΩ's resistance. Fig. 3 illustrates a basic concept of realizing the six kinds of resistance values.

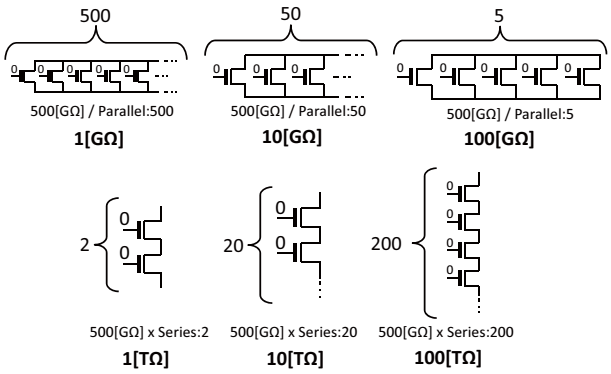

Fig. 3. How to configure a huge resistance

In addition, as a condition for obtaining a stable gate-off resistance of 500 GΩ, the MOSFET must always satisfy $V_{gs} = 0$. Assuming that 0 V is applied to the MOSFET's V_g from the outside, $V_{gs} = 0$ can not be satisfied if the fluctuation exists in V_s. However, as shown in Fig. 1, the I-V conversion circuit always has 0 V at the input V_{in}^- by the virtual ground. Observing Fig. 2, therefore, even if there is some input offset voltage in the op-amp, a constant resistance value can be obtained unless V_{gs} exceeds about 200 mV.

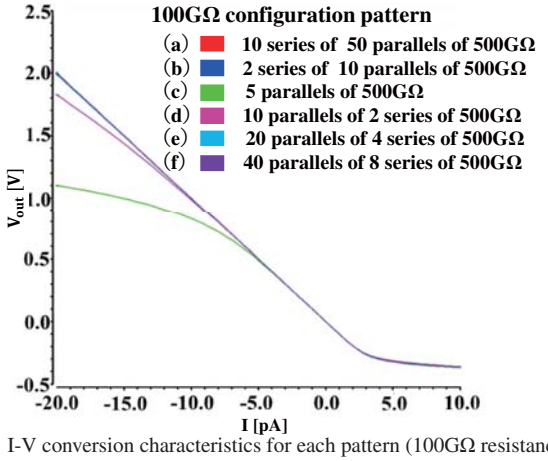

Fig. 4. I-V conversion characteristics for each pattern (100GΩ resistance)

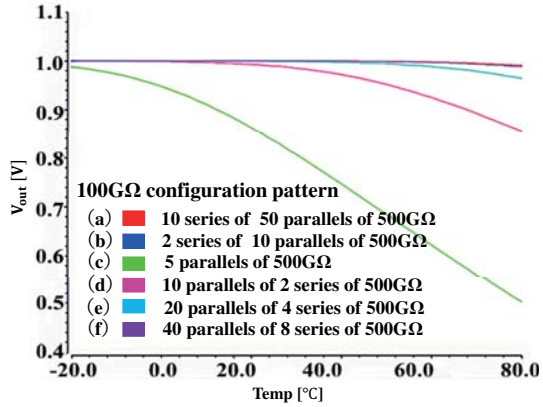

Fig. 5. Temperature characteristics for each pattern (100GΩ resistance)

TABLE I
CONFIGURATION OF EACH RESISTANCE

resistance	configuration	MOSFETs
1G	1000 parallels of 2 series	2000
10G	200 parallels of 4 series	800
100G	10 series of 50 parallels	500
1T	10 series of 5 parallels	50
10T	20 series	20
100T	200 series	200

D. Number of MOSFETs in Parallel and in Series

We present, taking 100 GΩ as an example, a more precise configuration pattern of resistance. The configuration patterns of different connections are as Fig.4,Fig.5.

We compare each pattern by simulation with respect to I-V conversion characteristic and temperature characteristic. The simulation results implies pattern (a) is most appropriate. It can be observed that the characteristics improves as the number of transistors increases in the simulation results. Note that, patterns (b) and (d) obtain completely equal simulation results. This is because the number of transistors is equal. Therefore, it is considered to be dominantly affected by the number of transistors regardless of the number of parallels and the number of series. We analogously verify the remaining 1 GΩ, 10 GΩ, 1 TΩ, 10 TΩ, 100 TΩ, then the optimum configuration patterns

TABLE II
I-V conversion characteristics and output range: Comparison between Poly resistance and suggested resistance

	Poly Resistance	1G	10G	100G	1T	10T	100T
Output Voltage(1[V])	999.934 [mV]	998.078 [mV] (−1[nA])	999.055 [mV] (−100[pA])	999.815 [mV] (−10[pA])	999.815 [mV] (−1[pA])	999.873 [mV] (−100[fA])	999.898 [mV] (−10[fA])
Offset Voltage(0[V])	38.173[μV]	30.946 [μV]	29.261 [μV]	28.308 [μV]	28.308 [μV]	27.997 [μV]	27.720 [μV]
Output Range : V (Error within 1%)	—	−0.143 [V] ~ 0.941 [V]	−0.133 [V] ~ 2.325 [V]	−0.127 [V] ~ 2.481 [V]	−0.127 [V] ~ 2.481 [V]	−0.125 [V] ~ 2.481 [V]	−0.124 [V] ~ 2.481 [V]
Output Range: I (Error within 1%)	—	0.143[nA] ~ − 0.951[nA]	13.473[pA] ~ −234.897[pA]	1.282[pA] ~ −25.000[pA]	0.128[pA] ~ −2.5000[pA]	12.633[fA] ~ −250.000[fA]	1.250[fA] ~ −25.000[fA]

are confirmed.

1. *I-V conversion characteristics:* Fig. 4 shows the simulation results when six types of resistance patterns of 100 GΩ are incorporated into the I-V conversion circuit and the input current is changed. Since the power supply of the op-amp is ±2.5 V, considering the range, the interval where the linearity is obtained in the input range of -20 pA to 10 pA is outputted. From the results, the linearity is obtained over a wide range in the order of (a), (f), and (e). As well, it is confirmed that the linearity from 0 pA to the minus direction is obtained. This linearity enables the MOSFET array to be used as a resistor with the range.

   Note that, as described above, since the current flows from 'WE' to 'CE' in the potentiostat, the linearity with respect to the current in the positive direction is not considered in this paper. The simulation setting is at room temperature 27° C.

2. *Temperature characteristics:* Fig. 5 shows the simulation result of the temperature characteristic of each resistance pattern when sweeping the temperature in the range of -20 to 80°C. The output voltage when the resistance pattern is connected to the I-V conversion circuit is measured. The input current is -10 pA. The temperature characteristic of the op-amp can be relatively ignored. The simulation results confirm us that the effects of temperature change on (a) and (f) are small.

We similarly verify the I-V characteristics and the temperature characteristics in 1 GΩ, 10 GΩ, 1 TΩ, 10 TΩ, 100 TΩ, and adopt the following configuration.

IV. Our On-chip Resistance Evaluation

For 1 GΩ - 100 TΩ, we compare the resistance of the configuration adopted in the previous section and the existing Poly resistance. The existing one is the HR-Poly resistance of the 0.6 μm process, where the sheet resistance (W/L=1.2/80.0) = 7000 (Ω/sq.), the resistance temperature coefficients are TC1 = -5.75E-03 (1/°C) and TC2=2.12E-05 ($1/°C^2$), and the resistance voltage coefficients are VC1 = -4.80E-04 (1/V) and VC2=-06 ($1/V^2$).

Table II summarizes results of finding the range within 1 % of the error against the existing Poly resistance by verifying the I-V conversion characteristic in the previous section. The simulation setting is at room temperature 27° C. Plus, the influence of the output on the temperature change of the proposed resistor is much smaller than the existing Poly resistance.

Table III shows the area comparison result. Although the area of the existing Poly resistor increases proportional to the resistance value, the area of the proposed resistor varies according to the number of transistors shown in Table I. As a result, the proposed resistor is much smaller as the resistance becomes particularly high.

TABLE III
Comparison of area

	Poly resistance[mm^2]	Our resistance[mm^2]
1G	1.279	0.228
10G	7.001	0.091
100G	70.741	0.053
1T	708.103	0.006
10T	7081.723	0.002
100T	70817.923	0.023

V. Conclusion

We propose on-chip high resistance employing the characteristics of subthreshold region of the MOSFET which is used in the current measurement circuit of the potentiostat method. We present the configuration of the specified resistance value by connecting unit resistor in parallel and in series, and suggest appropriate patterns for the range of the resistance according to the simulation results. The simulation results confirm us that the linearity of I-V conversion is obtained with an error of 1 % or less around 0 V-2.5 V in the potentiostat. Plus, the temperature characteristics of our proposed resistor is better than the existing Poly resistance for all resistance values, and the area can be drastically reduced at higher resistance. In future works, we will verify the circuit characteristics after the layout as well as an influence in PSRR.

References

[1] H. Katano, *Characteristics of electrochemical analysis method viewed from potentiostat*, Review of Polarography 2012.

[2] K. Ueno, T. Hirose, T. Asai, Y. Amemiya, *An Ultra-low Power Voltage Reference consisting of Subthreshold MOSFETs*, IEICE Tech. Rep., vol. 108, no. 253, ICD2008-68, pp. 55-60, Oct. 2008.