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A Global Buffer and Splitter Insertion Algorithm in AQFP Circuits	Rongliang Fu (The Chinese University of Hong Kong, Hong Kong), Mengmeng Wang (Yokohama National University, Japan), Yirong Kan (NARA Institute of Science and Technology, Japan), Olivia Chen (Tokyo City University, Japan), Nobuyuki Yoshikawa (Yokohama National University, Japan), Tsung-Yi Ho (The Chinese University of Hong Kong, Hong Kong)
A Scalable Linear Equation Solver FPGA using High-Level Synthesis	HAOPENG MENG, KAZUTOSHI WAKABAYASHI, TADAHIRO KURODA (The University of Tokyo, Japan)
A Study on Accurately Characterizing the Cells' Output Currents of a Read-Decoupled 8T SRAM Array for Computing-in-Memory Applications	Hao-Chiao Hong, Bo-Chang Chen (National Yang Ming Chiao Tung University, Taiwan)
A Study on the Design of Interface Circuits Between Synchronous-Asynchronous Modules Using Click Elements	Shogo Semba, Hiroshi Saito (The University of Aizu, Japan)
A Thermally Optimizing Method of Thin Film Resistor Trimming with Machine Learning	Tomoya Akasaka (Hirosaki University, Japan), Shigeru Hidaka (NiKKOHM.CO.,LTD, Japan), Ryosuke Watanabe, Taisei Arima, Atushi Kurokawa, Toshiki Kanamoto (Hirosaki University, Japan)
Aging-Compromised Computing-In-Memory Dot-Product Calculation Technique Through DVFS	Yu-Guang Chen, Chi-Hsu Wang (National Central University, Taiwan), Ing-Chao Lin (National Cheng Kung University, Taiwan)
An Efficient LSI Implementation of the Summation of Products in Convolution Operation for Binarized Neural Networks	Mitsuru Takahashi, Kazuhito Ito (Saitama University, Japan)
An Efficient Realization of Power-Root SC Calculations by Inserting Bits	Yuuto Arimura, Shigeru Yamashita (Ritsumeikan University, Japan)
An Error Diagnosis Technique Based on Location Variable Simulation Employing Implicit Representation of Error Location Sets	Hiroki Tsuyama, Akio Masamori, Nobutaka Kuroki, Masahiro Numa (Kobe University, Japan)
An Implementation of Self-Testable Layout-Level Scan C-element	Kokoro Yamasaki, Hiroshi Iwata, Ken'ichi Yamaguchi (National Institute of Technology, Nara College, Japan)
An NDA-free oriented Open PDK technology and EDA for small volume LSI developments	Seijiro Moriyama (Anagix Corporation, Japan), Tadaaki Tsuchiya, Shingo Ura (Logic Research Co., Ltd., Japan)
Binary Synthesis Using High-Level Synthesizer as its Back-End	Ryo Nakamichi, Sho Kishimoto, Nagisa Ishiura, Takumi Kondo (Kwansei Gakuin University, Japan)
Binding and Scheduling of 2̄3̄ Mixers for Transport-Free Sample Preparation Using Programmable Microfluidic Devices	Masataka Hirai, Shigeru Yamashita (Ritsumeikan University, Japan), Sudip Roy (Indian Institute of Technology (IIT) Roorkee, India), Hiroyuki Tomiyama (Ritsumeikan University, Japan)
Bottleneck Channel Routing to Reduce the Area of Analog VLSI	Kazuya TANIGUCHI, Satoshi TAYU, Atsushi TAKAHASHI (Tokyo Institute of Technology, Japan), Yukichi TODOROKI, Makoto MINAMI (Jedat, Japan)
Co-optimization of Prefix Structure and Bit-Line Arrangement for Long Bit-Length Parallel Prefix Adders	Kazuya Uryu, Mineo Kaneko (Japan Advanced Institute of Science and Technology, Japan)
Development of Diagnosis-based Hardware Trojan Tolerate System	Takuro Kasai, Masashi Imai (Hirosaki University, Japan)
Development of Text Translation System from Tsugaru Dialect into Common Japanese	Taiki Niida, Masashi Imai (Hirosaki University, Japan)
DNN-based Accelerator for Intelligent Robotic Arm Control with High-Level Synthesis	Yu-Chien Chung, Hao-Hsiang Lian, Yong-Lun Xiao, Chih-Tsun Huang, Jing-Jia Liou (National Tsing Hua University, Taiwan)
Efficient Hardware Architecture for Taylor-Series Expansion Calculation Using Distributed Arithmetic with Term Division	Xaybandith Hemthavy, Jianglin Wei, Shogo Katayama, Anna Kuwana, Haruo Kobayashi (Gunma University, Japan), Kazuyoshi Kubo (Oyama National College of Technology, Japan)
Electronic Component Placement Optimization for Heat Measures of Smartglasses	Kyosuke Kusumi (Hirosaki University, Japan), Koutaro Hachiya (Teikyo Heisei University, Japan), Ryotaro Kudo, Toshiki Kanamoto, Atsushi Kurokawa (Hirosaki University, Japan)
Evaluating Accuracy of Quantum Circuit Learning via Quantum Circuit Mapping	Nanao Segawa, Takashi Sato (Graduate School of Informatics, Kyoto University, Japan)
Extending Channel Routing Method for Two-Layer Routing Problem allowing for terminals placed within the	Kaito Ishigami, Kunihiro Fujiyoshi (Tokyo University of Agriculture and Technology, Japan)
Feasibility Study of DSP Block Mapping Algorithms for FPGAs Utilizing SAT-solver and Top-down ZDD Construction	Takuya Serizawa, Koyo Shibata (Ritsumeikan University, Japan), Takashi Imagawa (Meiji University, Japan), Hiroyuki Ochi (Ritsumeikan University, Japan)

Flat-Shape Capacitive Sensor of Droplet Contact-Angle for Electrowetting-on-Dielectric Microfluidic Systems	Tomohiro Kodaniguchi, Akira Tsuchiya, Toshiyuki Inoue, Keiji Kishine (The University of Shiga Prefecture, Japan)
Formulation of Maximum Independent Set Problem for Simulated Quantum Annealing Machine	Haruki Nakayama, Yukihide Kohira (The University of Aizu, Japan)
Full Hardware Implementation of RTOS-Based Systems Using General High-Level Synthesizer	Takuya Ando, Iori Muguruma, Yugo Ishii, Nagisa Ishiura (Kwansei Gakuin University, Japan), Hiroyuki Tomiyama (Ritsumeikan University, Japan), Hiroyuki Kanbara (ASTEM RI/Kyoto, Japan)
Hardware RTOS Services for Full Hardware Implementation of RTOS-Based Systems	Hiro Minamiguchi, Masaki Nakahara, Yugo Ishii, Yukino Shinohara, Iori Muguruma, Nagisa Ishiura (Kwansei Gakuin University, Japan)
Heating of Foreign Object in Inductive Wireless Charging	Issei Sato, Ryotaro Kudo, Toshiki Kanamoto (Hirosaki University, Japan), Koutaro Hachiya (Teikyo Heisei University, Japan), Shinsuke Kashiwazaki, Atsushi Kurokawa (Hirosaki University, Japan)
Importance Evaluation Methodology of FFs for Design Optimization of Approximate Computing Circuits	Jiaxuan LU, Yutaka MASUDA, Tohru ISHIHARA (Nagoya University, Japan)
ML-assisted Sizing Approach for Low-Voltage Circuits Considering Process Variation	Ling-Yen Song, Chih-Yun Chou, Tung-Chieh Kuo, Chien-Nan Jimmy Liu, Juinn-Dar Huang (Institute of Electronics, National Yang Ming Chiao Tung University, Taiwan)
On Providing Faster IR-Drop Forcast via SVM-Based Solutions	Ya-Ying Chien (NYCU, Taiwan), Chang-Tzu Lin (ITRI, Taiwan), Hung-Ming Chen (NYCU, Taiwan)
On Technology Remapping Approach Using Multi-Gate Functionality of Reconfigurable Cells for Post-Mask ECO	Tomohiro Nishiguchi, Nobutaka Kuroki, Masahiro Numa (Kobe University, Japan)
On-Interposer Decoupling Capacitors Placement for Interposer-based 3DIC	Po-Yang Chen, Chang-Yun Liu, Po-Tsang Huang, Hung-Ming Chen (NYCU, Taiwan)
Optimal Synthesis of NNA-Compliant Quantum Circuits in 2-D Architectures by Utilizing Don't Care Conditions	Kyohei Seino, Shigeru Yamashita (Ritsumeikan University, Japan)
PCB Component Copper Landing Pad Design Optimization	Hsiao-Chieh Ma, Yi-Yu Liu (National Taiwan University of Science and Technology, Taiwan)
Remote Access Tag Array for Efficient GPU Intra-Cluster Data Sharing	Bo-Wun Cheng, En-Ming Huang, Chen-Hao Chao, Wei-Fang Sun (National Tsing Hua University, Taiwan), Tsung-Tai Yeh (National Yang Ming Chiao Tung University, Taiwan), Chun-Yi Lee (National Tsing Hua University,
Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorted Alternately with Digital Method	Yi Liu, Anna Kuwana, Shogo Katayama, Xiongyan Li (Gunma University, Japan), Atsushi Motozawa (Renesas Electronics Corporation, Japan), Haruo Kobayashi (Gunma University, Japan)
SNRoverSDNN: A Metric for Robust CNN-based ROI Selection in Remote Heart Rate Extraction	Yuta Hitotsuyanagi, Takashi Sato (Graduate School of Informatics, Kyoto University, Japan)
Tag-less compression for FPGA configuration data	Souhei Takagi, Naoya Niwa, Yusuke Yanai, Hideharu Amano, Masaki Amagasaki (Keio University, Japan), Yuya Nakazato, Masahiro Iida (Graduated School of Advanced Science and Technology, Kumamoto, Japan)
Tail Layer CNN Training for a SoC-based FPGA	Yuki Takashima, Akira Jinguji, Ryosuke Kuramochi, Ryota Kayanoma, Hiroki Nakahara (Tokyo Institute of Technology, Japan)
Trotter Based Parallel Processing of Quantum Annealing for FPGA	Sohei Shimomai, Shinji Kimura (Waseda University, Japan)
Voice Learning of Reservoir Computing Architecture using Ternary Content Addressable Memory with Individuality	Sayaka Akiyama, Go Ajiki, Kong Xiangbo, Takeshi Kumaki (Ritsumeikan University, Japan)