Broadband 5G Millimeter-Wave Low Noise Amplifier (LNA) Design in 22 nm FD-SOI CMOS and 40 nm GaN HEMT

Clint Sweeney
ECE Dept.
Texas Tech University
Lubbock, TX, USA
clsweene@ttu.edu

Liang-Wei Ouyang
ECE Dept.
Texas Tech University
Lubbock, TX, USA
liang-wei.ouyang@ttu.edu

Donald Y.C. Lie
ECE Dept.
Texas Tech University
Lubbock, TX, USA
Donald.Lie@ttu.edu

Abstract - We present the design of two broadband millimeter-wave (mm-Wave) low noise amplifiers (LNAs) that cover the key 5G FR2 band in advanced semiconductor technologies. One LNA is designed with a 22 nm fully-depleted silicon-on-insulator (FD-SOI) CMOS and the other with a 40 nm GaN high-electron-mobility transistor (HEMT) process. Several post-layout parasitic extraction (PEX) options are compared vs. the EM (electromagnetic) simulations for the CMOS LNA design, while the EM PEX simulations are solely used for the GaN LNA design. The simulation data suggests both broadband LNAs are very competitive vs. state-of-the-art ones in literature. For example, the LNAs achieve 3-dB bandwidth (BW) of 16.9 – 41.8/19.8 – 43.1 GHz, and Noise Figure (*NF*) of 2.9 – 4.1/1.9-2.4 dB for the CMOS vs. GaN LNAs, respectively. When using a *FOM* (figure-of-merit) $\frac{OIP3*G*\mathrm{BW}}{(F-1)*\mathrm{Size}*P_{DC}}$ that accounts for linearity, power, *NF*, BW and size, both LNAs achieve among the best reported *FOM*s in literature.

I. Introduction

As 6G (sixth-generation) mobile technologies are being proposed with standards now under discussion, and 5G (fifth-generation) networks rolling out worldwide with increased popularity and performance, there is a great interest for broadband and highly power-efficient radio-frequency (RF) and millimeter-wave (mm-Wave) circuits and systems for commercial, civic and defense phased-array applications. For example, the 5G wireless revolution presents some dramatic challenges to the design of handsets and communication infrastructures, as 5G eMBB (enhanced Mobile Broadband) applications target 10-20 Gb/s download speeds and ×100 more wireless connected devices compared to 4G for mMTC (massive machine type communication) to realize Internet-of-Everything (IoE), and sub-1 mS latency time for UR/LL (ultra-reliable low latency) mMTC applications. However, to achieve all these goals for broadband wireless operation, it is necessary to move up from the sub-6 GHz 5G FR1 band to the millimeter-wave (mm-Wave) 5G FR2 Band (i.e., 24 – 52.6 GHz) to utilize more spectrum availability and multiple-input multiple-output (MIMO) antennas technologies. Furthermore, 6G targets aggressive peak data rate of 1 Tbps (i.e., ~ 50x of 5G), user-experienced data rate of 1 Gbps (i.e., ~ 10x of 5G), and latency of 0.1 ms (i.e., ~ 1/10x of 5G). A LNA is the first component in the receive (Rx) chain and it needs to be constantly turned on to listen and wake up the Rx and thus its *NF*, linearity, BW, power consumption, etc. are key to the overall performance of the RF front-end module (FEM) [1] and the success of a mm-Wave phased array system [2]. Wide bandgap semiconductor devices, such as gallium nitride (GaN) HEMTs, have shown great promise for low-noise and high-power mm-Wave LNAs due to their superior cut-off frequency f_T and breakdown performance vs. silicon-based LNAs [3-6]. However, silicon-based LNAs have benefitted from Moore's Law with excellent f_T lately, and their unparalleled integration capability with logics and control/memory circuits can achieve complex functionalities and smaller size for potential cost and form factor reduction [7-9]. The 22 nm FD-SOI CMOS technology is particularly interesting as it provides great integration potential for RF switches, PA (power amplifier), and LNA on the same die, and with very good substrate isolation, f_T and threshold voltage (V_T) adjustment by back-gate control [10-11]. Therefore, in this paper, we present and briefly compare two broadband mm-Wave LNA designs that cover the key 5G FR2 band: one in 22 nm FD-SOI CMOS and the other in 40 nm GaN/SiC HEMTs. Several post-layout parasitic extraction (PEX) options using Mentor/Siemens Calibre are compared vs. the EM simulation data for the CMOS LNA design, while only EM PEX simulations are used for the GaN LNA design. These two broadband LNAs show excellent *FOM*s for potential mm-Wave 5G FEM applications.

II. The Design of Broadband Mm-Wave LNAs

For each design, we checked to make sure the LNA is stable when biased at the operating points that we showed its post-PEX simulation data, and we also checked stability as the gate biasing was turned up (from cutoff up to the operating point). For the post-PEX simulation, Gamma probes were placed at the gates and drains of each stage to test the stability of the circuits internally (i.e., stability index, Nyquist stability criterion), and the K- and B-factors were checked to ensure the LNAs are unconditionally stable at their RF input and output.

A. Broadband LNA in 22FDX

The 22 nm FD-SOI CMOS (22FDX) technology from GlobalFoundries (GF) is used to design a single-ended 2-stage cascode-cascode mm-Wave broadband LNA. Devices achieve lower off-state leakage current due to the buried oxide layer and a fully depleted channel [7-9]. Our design uses SLVTNFET (i.e., super low threshold voltage NFET), which can achieve a peak f_T of ~350 GHz and a peak f_{MAX} of ~370 GHz in the smallest FETs [10-12].

Despite the benefits of increased BW and better input matching, noise from R_f and the reduced gain can deteriorate a LNA's *NF*. In pre-PEX simulations shown in Fig. 2, the optimal *NF* of the LNA can be matched near 2.4/2.8 dB before/after the resistive feedback is added. The PEX

simulations in Fig. 2(c) suggest only ~ 0.1 dB *NF* degradation from layout parasitics at 24 GHz. Fig. 3 shows the effects of 3 PEX options: R (resistance only), R+C (i.e., RC, resistance, capacitance to ground), and R+C+CC (i.e., RCC, resistance, capacitance to ground, and coupled capacitance) and compared them vs. pre-PEX simulations on *NF*, *S21* and *S11*.

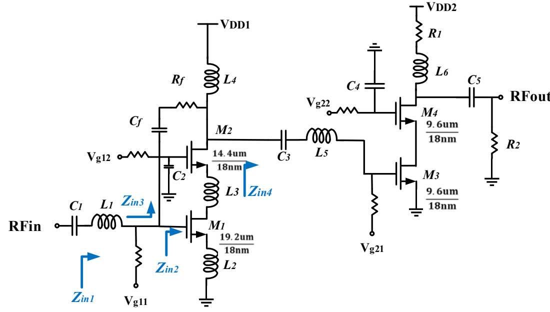


Fig. 1. Schematic of 2-stage LNA.

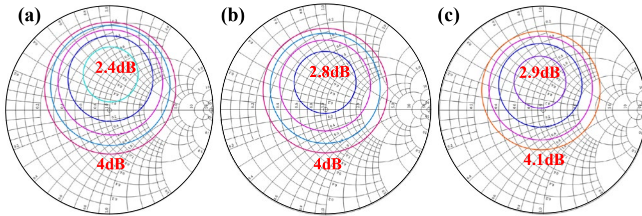
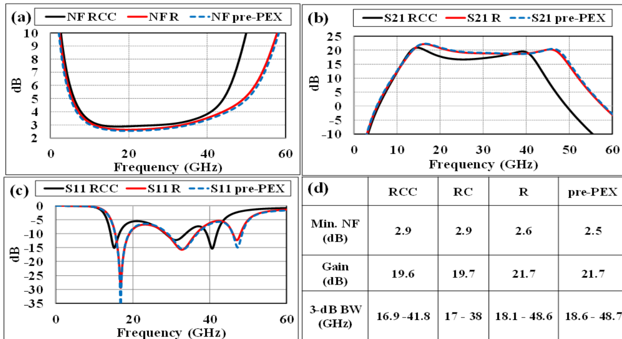
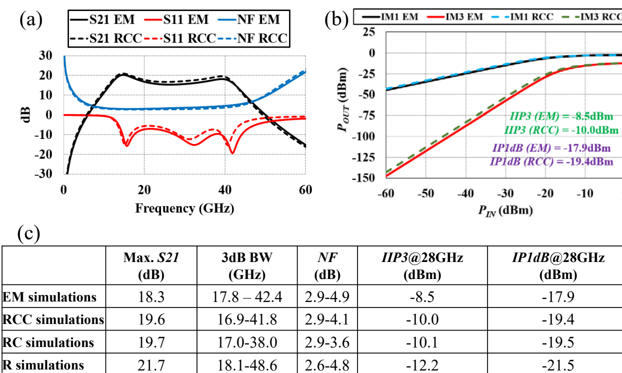


Fig. 2. Comparison of simulated noise circles of the LNA at 24 GHz: (a) without resistive feedback (pre-PEX); (b) with resistive feedback (pre-PEX); (c) with resistive feedback (PEX R+C+CC; or RCC).



	RCC	RC	R	pre-PEX
Min. NF (dB)	2.9	2.9	2.6	2.5
Gain (dB)	19.6	19.7	21.7	21.7
3-dB BW (GHz)	16.9 - 41.8	17 - 38	18.1 - 48.6	18.6 - 48.7

Fig. 3 PEX (RCC, RC, R) vs. pre-PEX simulations on (a) *NF*; (b) S_{21}; (c) S_{11}; (d) summary table.



	Max. *S21* (dB)	3dB BW (GHz)	*NF* (dB)	*IIP3*@28GHz (dBm)	*IP1dB*@28GHz (dBm)
EM simulations	18.3	17.8 – 42.4	2.9-4.9	-8.5	-17.9
RCC simulations	19.6	16.9-41.8	2.9-4.1	-10.0	-19.4
RC simulations	19.7	17.0-38.0	2.9-3.6	-10.1	-19.5
R simulations	21.7	18.1-48.6	2.6-4.8	-12.2	-21.5

Fig. 4 Comparison of PEX EM simulation vs. PEX RCC in (a) S_{21}, S_{11}, *NF* and (b) *IIP3* and IP_{1dB} at 28GHz (c) comparison table.

One can see once the parasitic capacitance is included, noticeable degradation on gain and BW are observed. When PEX EM simulations are used and compared vs. PEX RCC simulations, Fig. 4 shows that *S21*, *S11*, *NF* and *IIP3* and *IP1dB* all only changed within ~ 1.5 dB at 28 GHz, suggesting the faster PEX RCC simulations can be safely used in lieu of EM simulations for broadband mm-Wave LNA design.

B. Broadband LNA in 40 nm GaN HEMTs

Using the 40-nm T3 GaN technology from HRL Laboratories, a broadband 2-stage CS/2-stack LNA is designed to cover the key 5G FR2-band. The advanced low-voltage GaN technology has f_T >120 GHz and f_{max} > 240 GHz biased at the ~ 0.15 mA/µm, and its corresponding *NF* from 0.7 – 1 dB as in Fig. 5 [13-14]. Fig. 6 shows the schematics while Fig. 7 shows the large-signal PEX EM simulated performance.

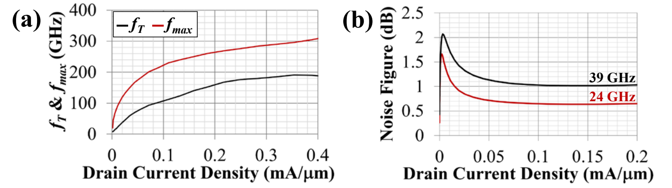


Fig. 5. Plots showing values of (a) f_T and f_{max} extrapolated from simulated AC current gain, $|H_{21}|$, and max. available gain, G_{max}, and (b) minimum *NF* vs. current density for 4x37.5-µm GaN devices.

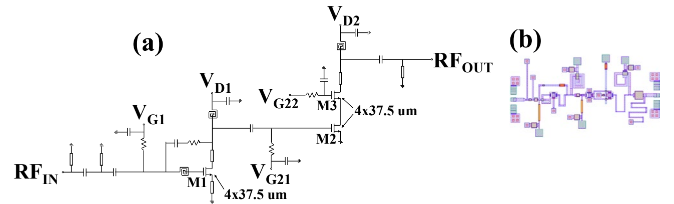


Fig. 6. (a) Schematic and (b) layout of the 2 x 1 mm² 2-stage GaN CS/2-stack LNA.

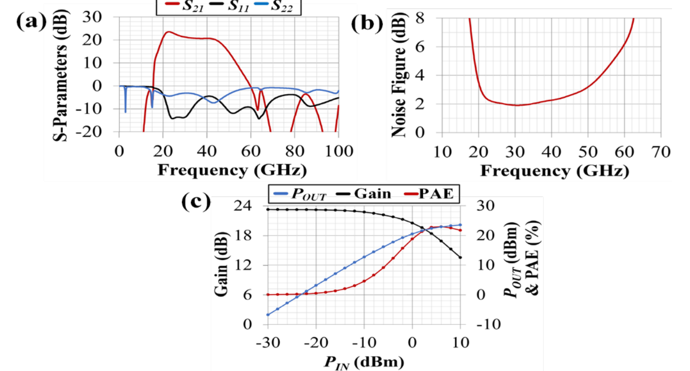


Fig. 7. PEX EM simulated (a) S-parameters, (b) *NF*, and (c) large signal at 24 GHz of the broadband CS/2-stack GaN LNA.

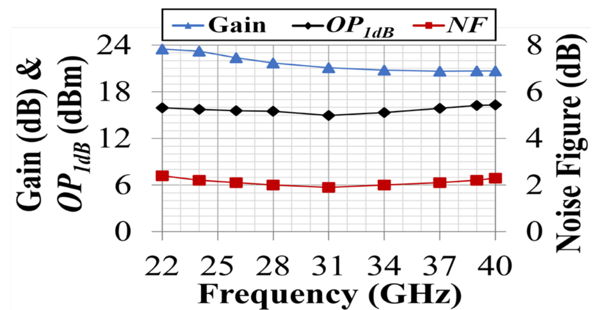


Fig. 8. PEX EM simulations of *NF*, gain and OP_{1dB} of the GaN LNA.

Using inductive source degeneration along with a series inductance on the gate of the 1st stage minimizes the LNA's *NF*, while a 2-stack 2nd stage help the gain to 20 dB [15-16].

III. Discussions and Conclusions

When designing a LNA for broadband mm-Wave phased array applications, its BW, linearity, *NF*, gain, power consumption and die size are all important. Therefore, we have come up with a *FOM* (figure-of-merit) = $\frac{OIP3*G*\text{BW}}{(F-1)*\text{Size}*P_{DC}}$ to compare our designs with the state-of-the-art broadband mm-Wave LNA reported in the literature. One can see from Table 1 both our LNAs have achieved among the best reported *FOMs* in literature. This is likely due to the advanced technology nodes we are using to design the LNAs with, together with the circuit topologies we have adopted, even though the results still need to be validated by measurement data after the chips are fabricated and tested. It is interesting to point out that, similar to many of the CMOS LNAs reported, our 22 nm CMOS FD-SOI LNA has very low power consumption and also lower linearity performance compared with the GaN LNAs. The GaN HEMTs intrinsically has much higher V_{DD} than nm-CMOS, so our GaN LNA has ~ x24 power consumption than our CMOS LNA, but it does have considerably higher linearity (~ 16 dB higher *OIP3*). However, using our proposed *FOM*, our GaN LNA still outperforms our CMOS LNA, suggesting this *FOM* can provide a reasonably fair assessment for broadband mm-Wave LNA performance, independent of the technologies used. Therefore, we hope this kind of technology-agnostic *FOM* may be useful to assist the synthesis for broadband LNA design automation in the future.

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References

[1] L. Letailleur *et al.*, IEEE INMMiC, Cardiff, UK, pp. 1-3, 2022.
[2] B. Sadhu et al., IEEE ISSCC Dig. Tech. Papers, San Francisco, CA, USA, pp. 436-438, 2022.
[3] X. Tong *et al., IEEE Microw. Wirel. Compon. Lett.*, vol. 30, no. 12, pp. 1153-1156, Dec. 2020.
[4] H. P. Moyer, A. Kurdoghlian, M. Micovic, T. Lee, and M. Hu, Proc. IEEE CSICS, Monterey, CA, USA, pp. 1–4, Oct. 2008.
[5] M. Sato et al., IEEE MTT-S Int. Microw. Symp. Dig., San Francisco, CA, USA, pp. 1–4, May 2016.
[6] M. Rudolph, N. Chaturvedi, K. Hirche, J. Wurfl, W. Heinrich and G. Trankle, *IEEE Microw. Wirel. Compon. Lett.*, vol. 19, no. 4, pp. 251-253, April 2009.
[7] Y. Hu and T. Chi, *IEEE Microw. Wirel. Compon. Lett.*, vol. 31, no. 6, pp. 725-728, June 2021.
[8] L. Gao and G. M. Rebeiz, Proc. IEEE RFIC Symp., Boston, MA, USA, pp. 239-242, 2019.
[9] O. El-Aassar and G. M. Rebeiz, *IEEE Trans. Microw. Theory Tech.*,, vol. 68, no. 10, pp. 4445-4454, Oct. 2020.
[10] www.globalfoundries.com/technology-solutions/cmos/fdx/22fdx
[11] J.C. Mayeda, D.Y.C. Lie and J. Lopez, Proc. IEEE ISCAS, May 26-29, Sapporo, Japan, 2019.
[12] L.-W. Ouyang *et al.*, Proc. IEEE IS3C, Taichung, Taiwan, June 30 - July 3, 2023
[13] https://www.hrl.com/tag/t3
[14] S. D. Burnham *et al.,* IEEE Trans. Semicond. Manuf., vol. 30, no. 4, pp. 480-485, Nov. 2017.
[15] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi and P. M. Asbeck, *IEEE Trans. Microw. Theory Tech.,* vol. 58, no. 1, pp. 57-64, Jan. 2010.
[16] C. Sweeney, J.C. Mayeda, D.Y.C. Lie and J. Lopez, Proc. IEEE ICEIB, Taichung, Taiwan, April 14-16, 2023.

TABLE I PERFORMANCE COMPARISON OF STATE-OF-THE-ART BROADBAND MILLIMETER AND/OR KA-BAND LNAS

Ref.	Tech.	Design	DC P_{DC} (W)	3-dB BW from Max. Small Signal Gain (GHz)	Max. Small Signal Gain, *G* (dB)	*NF* (dB)	Core size (mm^2)	OP_{1dB} (dBm)	**Max. *FOM*** $\frac{OIP3*G*BW}{(F-1)*Size*P_{DC}} * 10^{-6}$
[1]	40-nm GaN-SiC	3-stage CS	0.5	24.3-29.5	18.3-20.2	2.5-3.1	3.8	8.3	0.02
[3]	0.1-μm GaN-Si	4-stage CS/Cascode	1.4	18-56	16-21.5	2.2-4.4	4.8	10-20	1.2
[4]	0.15-μm GaN-SiC	3-stage CS	0.4	42-47	19-20	2.9-3.7	3.3	26-28	2.5
[5]	0.12-μm GaN-SiC	2-stage CG	0.28	33-41	12-15	3-4	0.7	13-24	3.3
[6]	0.15-μm GaN-SiC	4-stage CS	0.56	27-31	12	3.7-3.9	4.1	N/A	N/A
[7]	45-nm CMOS RFSOI	2-stage Cascode	0.026	25.5-50	21.2	2.4-4.2	0.38	-0.4	4.0
[8]	22-nm CMOS FDSOI	3-stage Cascode	0.025	24-43	23	3.1-3.7	0.21	1.6	10.0
[9]	22-nm CMOS FDSOI	1-stage CS	0.015	21.6-32.8	10.2	2.2	0.12	6.2	4.1
EM Sim. Only Our Lab [12]	22-nm CMOS FDSOI	2-stage Cascode	0.016	16.9-41.8	19.6	2.9-4.1	0.24	-0.8	5.2
EM Sim. Only This Work	40-nm GaN-SiC	2-stage CS/2stack	0.38	19.8-43.1	20.6-23.6	1.9-2.4	2	15-16.3	5.5

**OIP3* is estimated as OP_{1dB} + 10 in dBm, and *F* is the non-dB form of *NF*
***OIP3*, *G* and P_{DC} are used in their non-dB form for the *FOM* calculation
***BW is used as the absolute BW for the *FOM* calculation