

A Fast Three-layer Bottleneck Channel Track Assignment with Layout Constraints using ILP

Kazuya TANIGUCHI Satoshi TAYU
Atsushi TAKAHASHI

Department of Information and Communications Engineering
Tokyo Institute of Technology
2-12-1 S3-58 Ookayama, Meguro-ku, Tokyo 152-8550, Japan
{taniguchi@eda., tayu@, atsushi@}ict.e.titech.ac.jp

Mathieu MOLONGO Makoto MINAMI
Katsuya NISHIOKA

Jedat
1-1-12, Minato, Chuo-ku, Tokyo 104-0043, Japan
{molongo.mathieu, minami.makoto,
nishioka.katsuya}@jedat.co.jp

Abstract— An algorithm for a bottleneck channel routing problem that uses ILP is proposed. The proposed algorithm determines the track and layer assignment of nets for three-layer bottleneck channel routing problem with layout constraints in which pins of each net are placed on the upper boundary of the adjacent regions on both sides of the bottleneck channel. The proposed algorithm restricts the routing pattern of each net to one of three patterns by taking feasibility into account, and outputs a solution in a few seconds when the number of nets is 300.

I. INTRODUCTION

The analog layout design is required not to deteriorate the circuit performance. On the other hand, it is important to realize a layout in a small area to reduce manufacturing costs. The objective of our research is to develop a routing framework that enables us to layout a circuit in small area while meeting performance specifications.

In this paper, a routing problem on the bottleneck routing region where performance specifications are not violated even if multiple wires go through a track is discussed.

For routing problems which contain layout constraints, it is not easy to construct constructive algorithms that consider all constraints. If the routing problem can be formulated as an Integer Linear Programming (ILP), layout constraints can be considered more easily than constructive algorithms. However, ILP is generally NP-hard and often difficult to solve in practical time, even for small-scale problems.

In cell-based design [1], the routing area is partitioned into small routing regions, and various routing algorithms for such regions have been proposed. For example, channel routing algorithms were proposed in [2, 3]. Track assignment procedure considering cross-talk minimization was proposed in [4]. A design flow without repeating design is preferred [5, 6, 7]. A routing design flow with HV routing without repeating routing design has been established. However, the obtained layout may contain a

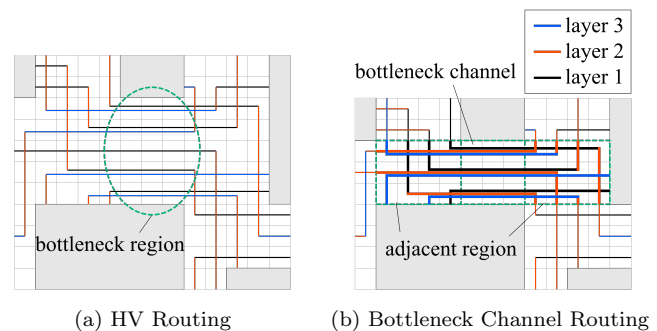


Fig. 1. Circuit layouts without and with bottleneck channel

routing region which is a bottleneck for area reduction (Fig. 1(a)). In order to resolve bottleneck, *Bottleneck channel routing* (Fig. 1(b)) is proposed in [8].

In this paper, we propose U3TLA-ILP3.0 that determines the track and layer assignment of nets by using ILP for U-shaped three-layer bottleneck channel routing problem (U3BCRP). A layout pattern obtained by using U3TLA-ILP3.0 will be utilized as an initial solution to explore a detailed routing in bottleneck region with layout constraints efficiently.

U3TLA-ILP3.0 restricts the routing pattern of each net to one of three patterns by taking feasibility into account. In U3TLA-ILP3.0, decision variables are used to determine the pattern used by each net, the track and layer assignment is determined according to the decision variables, and the routing pattern is determined. U3TLA-ILP3.0 outputs solutions in a few seconds for medium-scale problems about 300 nets. The routing pattern that satisfies layout constraints can be obtained in a short time by U3TLA-ILP3.0.

II. BOTTLENECK CHANNEL ROUTING PROBLEM

A routing problem is to find a better routing pattern that satisfies the connection requirement under the design rule. The connection requirement among pins is called a *net*. Among routing patterns which satisfy connection requirement, a routing pattern is *infeasible* if there is a

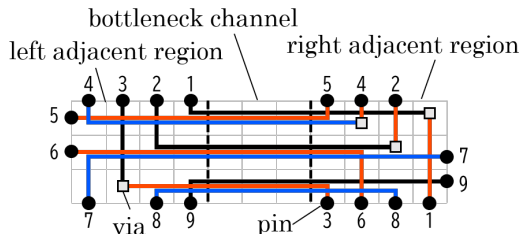


Fig. 2. Bottleneck channel routing

design rule violation, *feasible* otherwise.

In grid based design, the wires of different nets have a *conflict* if they share the same coordinate in the same layer. In grid based design, a solution which satisfies connection requirement and have no conflicts is feasible. The solution of a routing problem must be feasible and must meet layout constraints.

Three-layer bottleneck channel routing problem is defined on routing area that consists of a *bottleneck channel* and *adjacent regions* on both sides as shown in Fig. 2. A wire which connects pins of a net goes through a track in the bottleneck channel. A set of two-pin nets $N = \{n_1, n_2, \dots, n_k\}$ is given as an input. Pins of each net are placed on the boundary of left and right adjacent regions. The left sequence $L = (l_1, l_2, \dots, l_k)$ where $l_i \in N$ is defined as the sequence of nets whose pins are aligned counterclockwise order on the boundary of the left-adjacent region. Similarly, the right sequence $R = (r_1, r_2, \dots, r_k)$ where $r_i \in N$ is defined as the sequence of nets whose pins are aligned clockwise order on the boundary of the right-adjacent region. $N^l(n)$ and $N^r(n)$ are the sets of nets whose left and right pins are before the left pin and the right pin of net n in the left and right sequences, respectively. That is, they are defined as

$$N^l(n) = \{l_i \mid i < j, n = l_j\}, \quad (1)$$

$$N^r(n) = \{r_i \mid i < j, n = r_j\}. \quad (2)$$

In this paper, U-shaped three-layer bottleneck channel routing problem (U3BCRP) shown in Fig. 3 which is the most basic three-layer bottleneck channel routing problem is formulated. In U3BCRP, routing area $G_{k,T}$ for k two-pin nets and T tracks is modeled by the routing grid $(-k \leq x \leq k, 0 \leq y \leq T)$ as shown in Fig. 4 where the y -axis corresponds to the degenerated bottleneck channel, the region $x < 0$ corresponds to the left-adjacent region, and the region $x > 0$ corresponds to the right-adjacent region. Left pin of net l_i and right pin of net r_j are placed at grid point $(-i, 0)$ and $(j, 0)$, respectively. Track t ($1 \leq t \leq T$) is the grid line connecting $(-k, t)$ and (k, t) .

Wires of at most three nets can go through a single track. In the following, we assume that an input which satisfies

$$k \leq 3T \quad (3)$$

is given. Also, we assume, without loss of generality, that left sequence L is fixed as $l_i = n_i$ for any net $n_i \in N$.

U3BCRP

Input:

- net set $N = \{n_1, n_2, \dots, n_k\}$ ($k > 0$)
- right sequence $R = (r_1, r_2, \dots, r_k)$
- the number of tracks $T \in \mathbb{N}^+$

Output:

- track assignment of nets
 $A_T : N \rightarrow \{1, 2, \dots, T\}$
- layer assignment of segments of nets
 $A_L : N \rightarrow \{1, 2, 3\}$ (left vertical)
 $A_M : N \rightarrow \{1, 2, 3\}$ (horizontal)
 $A_R : N \rightarrow \{1, 2, 3\}$ (right vertical)

Fig. 3. U-shaped three-layer bottleneck channel routing problem

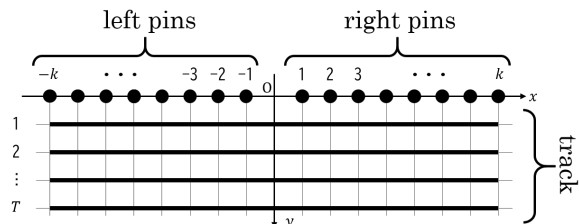


Fig. 4. Routing area $G_{k,T}$, tracks, and pins

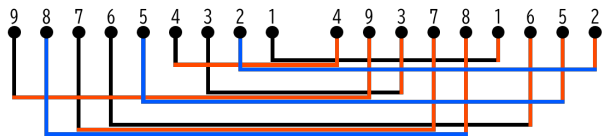


Fig. 5. A routing pattern for $R = (n_4, n_9, n_3, n_7, n_8, n_1, n_6, n_5, n_2)$

Therefore, right sequence R is given as input. In addition, we assume that layout constraints may be given, such as wires of two specified nets must not be close to each other.

In U3BCRP, an output routing pattern has to satisfy the following four conditions.

- Pin of all nets are connected by wire.
- Wires of different nets have no conflicts.
- The wire of each net consists of one horizontal and two vertical segments.
- Each segment is assigned to either layer 1, 2, or 3.

The wire of a net consists of two vertical segments and one horizontal segment which is assigned to a track.

Output of the problem is the track assignment A_T and the layer assignment of three segments A_L , A_M , and A_R . The routing pattern is uniquely determined under the four conditions above if the track and layer assignment is determined. If the wires of different nets share the same coordinate, they must be assigned to the different layer to avoid conflicts.

Once the track assignment $A_T(n)$ is determined, the track used by the horizontal segment of net n and the length of the vertical segments of net n are determined, and the routing shape of net n is determined.

Fig. 5 shows an example of routing pattern. The black, red, and blue line segments represent the wires on layer 1, layer 2, and layer 3, respectively.

For each net, via must be inserted to a wire when the routing layer of the wire is changed. A via placed between layer i and layer j is called i - j via. A conflict occurs when a 1-3 via and a wire on layer 2 share the same coordinate. Note that a 1-2 via can share the same coordinate with a wire on layer 3 without conflict.

III. TRACK ASSIGNMENT TO AVOID CONFLICT

Before introducing ILP formulations for U3BCRP, necessary conditions in track assignment to avoid conflicts when the routing layer of each segment of nets is specified are discussed.

Let $N_{i,i}$ be the set of nets whose left vertical segment and horizontal segment both use layer i . All horizontal segments of nets belonging to $N_{i,i}$ use the layer i , and all nets belonging to $N_{i,i}$ are assigned to different tracks if the routing pattern has no conflicts. Let a and b be nets belonging to $N_{i,i}$ such that $a \in N^l(b)$. If net a is assigned to a track below the track to which net b is assigned, the left vertical segment of net a and the horizontal segment of net b intersect on the same layer, and conflict occurs as shown in Fig. 6(a). To avoid the conflict between net a and net b , net a must be assigned to a track above the track to which net b is assigned as shown in Fig. 6(b).

If a routing pattern contains no conflicts, all nets belonging to $N_{i,i} \cap N^l(n)$ are assigned to a track above the track to which net $n (\in N_{i,i})$ is assigned. In this situation, the following equation holds.

$$\forall n \in N_{i,i}, A_T(n) > |N_{i,i} \cap N^l(n)| \quad (4)$$

If a track assignment satisfies the condition of Eq. (4), the left vertical segment and the horizontal segment of nets belonging to $N_{i,i}$ have no conflicts.

IV. ILP FORMULATION WHICH REQUIRES MUCH CALCULATION TIME

In this section, a straightforward ILP formulation for U3BCRP is introduced. This formulation is natural and intuitive but impractical.

Fig. 7 gives a part of ILP formulation U3TLA-TLLL for U3BCRP. Since the logical product (\wedge) can be converted to an equivalent linear expression using auxiliary variables, a formulation which contains logical product is used here for clarity.

U3TLA-TLLL represents the routing of each net by using four variables defined in Eqs. (5), (6) which specify the track assignment and the layer assignment of three segments. $x_{t,n}^T$ specifies track assignment A_T . The net n is assigned to track t if $x_{t,n}^T = 1$. $x_{i,n}^L$, $x_{i,n}^M$, and $x_{i,n}^R$ specify layer assignment A_L , A_M , and A_R , respectively. For example, the left vertical segment of net n is assigned to layer i if $x_{i,n}^L = 1$.

In U3BCRP, each net is assigned to one track and each segment of a net uses one layer. They are forced by



Fig. 6. Track assignment with and without conflict

U3TLA-TLLL

Decision variables

$$x_{t,n}^T \in \{0, 1\} \quad (\forall (t, n) \in \{1, 2, \dots, T\} \times N) \quad (5)$$

$$x_{i,n}^L, x_{i,n}^M, x_{i,n}^R \in \{0, 1\} \quad (\forall (i, n) \in \{1, 2, 3\} \times N) \quad (6)$$

Constraints

- Pattern
$$\sum_{t=1}^T x_{t,n}^T = 1 \quad (\forall n \in N) \quad (7)$$

$$\sum_{i=1}^3 x_{i,n}^L = \sum_{i=1}^3 x_{i,n}^M = \sum_{i=1}^3 x_{i,n}^R = 1 \quad (\forall n \in N) \quad (8)$$
- Conflict
$$\sum_{n \in N} x_{t,n}^T \wedge x_{i,n}^M \leq 1 \quad (\forall t \in [T], \forall i \in \{1, 2, 3\}) \quad (9)$$

$$\sum_{t=1}^T t \cdot x_{t,n}^T < \sum_{t=1}^T t \cdot x_{t,n'}^T + T(1 - \sum_{i=1}^3 x_{i,n}^L \wedge x_{i,n'}^M) \quad (\forall (n, n') \in N^2, n \in N^l(n')) \quad (10)$$

$$x_{t,n}^T \wedge x_{t,n'}^T \wedge x_{2,n}^M \wedge x_{1,n'}^L \wedge x_{3,n'}^M = 0$$

$$x_{t,n}^T \wedge x_{t,n'}^T \wedge x_{2,n}^M \wedge x_{3,n'}^L \wedge x_{1,n'}^M = 0$$

$$(\forall (t, n, n') \in [T] \times N \times N, n' \in N^l(n)) \quad (11)$$

Fig. 7. ILP formulation U3TLA-TLLL

Constraint on Pattern in U3TLA-TLLL (Eqs. (7), (8)). The conflicts between the wires of different nets (Eqs.(9), (10)), and the conflicts between the 1-3 via and the wire on layer 2 (Eq. (11)) on left region are prohibited in the Constraint on Conflict in U3TLA-TLLL. The conflict on right region can be prohibited similarly, but the description is omitted here.

V. PROPOSED METHOD U3TLA-ILP3.0

In this section, the proposed algorithm for U3BCRP with ILP formulation U3TLA-ILP3.0 shown in Fig. 8 is introduced.

A. Routing pattern

U3TLA-ILP3.0 restricts the layer assignment of each net to three patterns shown in Fig. 9. U3TLA-ILP3.0 uses a variable that specifies the pattern used by each net, but does not use variables for track assignment.

The variables used in U3TLA-ILP3.0 are

$$p_n^i := \begin{cases} 1 & (\text{net } n \text{ uses } P_i) \\ 0 & (\text{otherwise}) \end{cases} \quad (12)$$

where $i \in \{1, 2, 3\}$ and $n \in N$. The net n uses P_i if $p_n^i = 1$. The Constraint on Pattern

$$p_n^1 + p_n^2 + p_n^3 = 1 \quad (\forall n \in N) \quad (13)$$

restricts the pattern of each net to one of three patterns.

B. Track Assignment

Proposed algorithm determines track assignment according to the patterns of nets determined by U3TLA-ILP3.0.

When all variables are determined to satisfy Eq. (13), the track assignment of net n using P_1 is defined as follows (see also Fig. 10).

$$A_T(n) := \sum_{m \in N^l(n)} p_m^1 + 1 \quad (14)$$

Note that $\sum_{m \in N^l(n)} p_m^1$ is equal to the number of nets which appear before n in the left-sequence L and that use P_1 . Both the left vertical segments and the horizontal segments of nets using P_1 use layer 1, and there is no conflict among them since the track assignments defined by Eq. (14) satisfy the condition of Eq. (4). The right vertical segments and the horizontal segments of nets using P_1 have no conflicts among them since the former use layer 2 and the latter use layer 1. Therefore, any nets using P_1 have no conflicts among them.

For any nets using P_2 (or P_3), the track assignments of nets are defined similarly so that they have no conflicts among them. Therefore, any nets using the same pattern have no conflicts.

The number of nets to be used for each pattern is less than or equal to the number of tracks T . The Constraint on Tracks

$$\sum_{n \in N} p_n^i \leq T \quad (\forall i \in \{1, 2, 3\}) \quad (15)$$

restricts the number of nets to be used for each pattern.

C. Constraints in ILP to avoid conflicts

From the restriction of routing pattern and the track assignment, any nets using the same pattern have no conflicts. A conflict occurs only if a vertical segment and a horizontal segment belong to different patterns. U3TLA-ILP3.0 imposes constraints which prevent conflicts caused by such segments belonging to different patterns.

For any pattern P_i , a conflict occurs when a vertical segment of P_i intersects the horizontal segment of other pattern $P_j (\neq P_i)$ which use the same layer. Among 12 pairs of vertical and horizontal segments belonging to different patterns, the following three are pairs of segments which use the same layer.

- right vertical segment of P_1 , horizontal segment of P_2
- left vertical segment of P_2 , horizontal segment of P_1
- right vertical segment of P_3 , horizontal segment of P_2

The intersection of segments in these three pairs are prohibited by the Constraint on Conflict shown below. The variable M used in these constraints is a big-constant defined as $M := T + 1$.

Algorithm for U3BCRP

Input: N

Output: $A_T(N), A_L(N), A_M(N), A_R(N)$

***** 1. Pattern selection using ILP *****

$P(p)$: ILP-formulation

Variables: Eq. (12)

Constraints

- Pattern: Eq. (13)
- Tracks: Eq. (15)
- Conflicts: Eq. (16, 17, 18)
- Layout: Eq. (21)

solve($P(p)$)

for($n \in N$)

$$p(n) := \begin{cases} 1 & \text{if } p_n^1 = 1 \\ 2 & \text{if } p_n^2 = 1 \\ 3 & \text{if } p_n^3 = 1 \end{cases}$$

endfor

***** 2. Track and layer assignment *****

for($n \in N$)

switch($p(n)$)

case(1):

$$A_T(n) := |\{m \mid m \in N^l(n), p(m) = 1\}| + 1$$

$$(A_L(n), A_M(n), A_R(n)) := (1, 1, 2)$$

case(2):

$$A_T(n) := |\{m \mid m \in N^r(n), p(m) = 2\}| + 1$$

$$(A_L(n), A_M(n), A_R(n)) := (1, 2, 2)$$

case(3):

$$A_T(n) := |\{m \mid m \in N^l(n), p(m) = 3\}| + 1$$

$$(A_L(n), A_M(n), A_R(n)) := (3, 3, 2)$$

endswitch

endfor

Fig. 8. Proposed Algorithm for U3BCRP

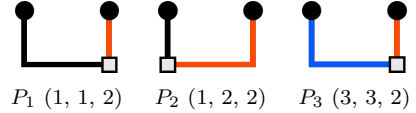


Fig. 9. Three patterns used by U3TLA-ILP3.0

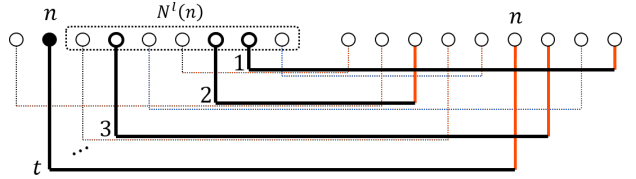


Fig. 10. Track assignment of P_1

$$\sum_{m \in N^l(n)} p_m^1 < \sum_{m \in N^r(n)} p_m^2 + M(1 - p_n^1) \quad (\forall n \in N) \quad (16)$$

$$\sum_{m \in N^r(n)} p_m^2 < \sum_{m \in N^l(n)} p_m^1 + M(1 - p_n^2) \quad (\forall n \in N) \quad (17)$$

$$\sum_{m \in N^l(n)} p_m^3 < \sum_{m \in N^r(n)} p_m^2 + M(1 - p_n^3) \quad (\forall n \in N) \quad (18)$$

In the following, we show that a conflict caused by segments belonging to different patterns are prohibited either

by Eqs. (16), (17), or (18). The value of each term in each formula is nonnegative, and the value of the left side is at most T in each formula. Therefore, note that an inequality is satisfied when $p_n^i (i = 1, 2, 3)$ is 0 since the value of the right side is at least $M (= T + 1)$. Also, Eqs. (16), (17), and (18) may not be satisfied when p_n^1 , p_n^2 , and p_n^3 are 1, respectively.

Here, we show that the left vertical segment of nets using P_2 and the horizontal segments of nets using P_1 do not intersect if Eq. (17) is satisfied. Let's consider a case that net n uses pattern P_2 , that is, $p_n^2 = 1$. We show that the left vertical segment of net n and the horizontal segments of nets using P_1 do not intersect if Eq. (17) is satisfied.

Let t be the value on the left side of Eq. (17).

$$\sum_{m \in N^r(n)} p_m^2 = t \quad (19)$$

From Eq. (14), $t+1$ is equal to the track number of net n . The left vertical segment of net n on layer 1 spans from track 1 to track $t+1$ as shown in Figs. 11 and 12. Let c be the value of the first term on the right side of Eq. (17).

$$\sum_{m \in N^l(n)} p_m^1 = c \quad (20)$$

Note that c represents the number of nets using P_1 which appear before net n in the left-sequence L . The horizontal segments of these nets terminate to the right of the left vertical segment of net n as shown in Figs. 11 and 12.

Note that $t < c$ holds if Eq. (17) is satisfied. If $t < c$, the horizontal segments of all nets using P_1 which are assigned to track 1 to track $t+1$ terminate to the right of the left vertical segment of net n as shown in Fig. 11. The left vertical segment of net n and the horizontal segments of nets using P_1 do not intersect, and no conflict occurs.

If $t \geq c$, conflict may occur as shown in Fig. 12. Suppose there exists a net n' which appear first in left-sequence L among nets using P_1 and whose left pin is to the left of that of net n . The net n' is assigned to track $c+1 (\leq t+1)$, and the horizontal segment of net n' on layer 1 terminates to the left of the left vertical segment of net n . The left vertical segment of net n and the horizontal segments of net n' intersect, and conflict occurs.

In summary, Eq. (17) restricts to $t < c$, and prohibit the intersection of the left vertical segment of nets using P_2 and the horizontal segments of nets using P_1 .

It can be shown similarly that the conflict between P_1 and P_2 and the conflict between P_3 and P_2 do not occur if Eqs. (16) and (18) are satisfied, respectively, but the description is omitted here.

D. Constraints in ILP to satisfy layout constraints

Among various types of layout constraints, ILP formulation that prevents crosstalk noise is discussed here as an example.

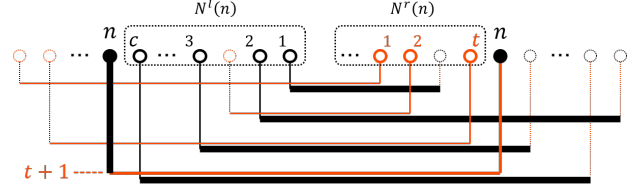


Fig. 11. No conflict at left vertical segment of P_2 ($t < c$)

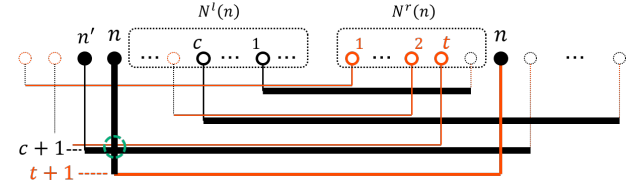


Fig. 12. Conflict at left vertical segment of P_2 ($t \geq c$)

Assume that a pair of a noise source *aggressor* and its *victim* are given, and that the wire of the aggressor and a victim neither share the same coordinate nor adjacent is requested even if they are assigned in different layer is given as constraint.

Let n_a be the aggressor, and let n_v be the victim. If the input satisfies both $n_a \in N^l(n_v)$ and $n_v \in N^r(n_a)$, the wires of n_a and n_v must intersect and no feasible solution exists. So we focus on the other situations. Suppose, without loss of generality, that an input which satisfies $n_a \in N^l(n_v) \cap N^r(n_v)$ is given. In order to satisfy the layout constraints, net n_a must be assigned to two or more tracks above the track to which n_v is assigned, regardless of patterns of them used.

The Constraints on Layout

$$\sum_{m \in N_i(n_a)} p_m^i \leq \sum_{m \in N_j(n_v)} p_m^j + (M+1)(2 - p_{n_a}^i - p_{n_v}^j) - 2 \quad (21)$$

$$\left(N_i(n) := \begin{cases} N^l(n) & (i = 1, 3) \\ N^r(n) & (i = 2) \end{cases} \right)$$

where $(i, j) \in \{1, 2, 3\}^2$ prohibit the intersection of the wires of n_a and n_v and secure the gap between the wires of them two tracks or more. The first term on the left and right sides represent the (track number)−1 of n_a and n_v , respectively. Note that Eq. (21) for (i, j) is satisfied if either $p_{n_a}^i = 0$ or $p_{n_v}^j = 0$ because of the second term on the right side.

In case that $p_{n_a}^i = 1$ and $p_{n_v}^j = 1$, the second term on the right side of Eq. (21) is zero, and Eq. (21) forces that

$$(\text{track number of } n_a) \leq (\text{track number of } n_v) - 2.$$

By the Eq. (21), net n_a is assigned to two or more tracks above the track to which n_v is assigned.

The Constraint on Layout given here is for a single pair of aggressor and victim, but the number of pairs is often more than one in practice. If more than one pairs are given, the layout constraints can be realized by adding constraint given here for each pair. Even if any other

layout constraint is given, a routing pattern which satisfies the constraint can be obtained if the constraint can be expressed in a linear equation.

E. Proposed Algorithm

Propose algorithm shown in Fig. 8 first formulates U3BCRP as U3TLA-ILP3.0. Proposed algorithm then solves the ILP using a solver to determine the pattern of each net.

Once the pattern of each net is determined, the track and layer assignment is determined uniquely. The track number of net n is set equal to the number of nets which appear before n in left or right sequence and which use the same pattern with n .

VI. EXPERIMENTAL RESULTS

U3TLA-ILP3.0 is implemented in Python 3.10.11, and executed on a PC with 3.60GHz Intel Core-i5 CPU, 32GB RAM. The solver used is IBM CPLEX 22.1.1.0.

The problem instances are randomly generated by selecting the right pin sequence among a permutation of nets. The number of nets k is set to be three times the number of tracks T . The symbol “*” is added when a layout constraint to prevent crosstalk in which a pair of one aggressor and 5 victims is defined is imposed to the problem instances. A routing pattern obtained by using U3TLA-ILP3.0 is shown in Fig. 13.

Table I shows the computation times of U3TLA-TLLL and U3TLA-ILP3.0 for various net sizes when a feasible solution is obtained. In table, “time” represents the computation time taken to solve the formulated ILP for one problem instance.

Table II shows the average computation times of U3TLA-ILP3.0 and the ratio that feasible solution is obtained among 100 problem instances for each net size. The ratio is reasonable since U3TLA-ILP3.0 cannot obtain a feasible solution if the first net in the right pin sequence is n_1 . Even in such cases, pre-processing, such as connecting net n_1 using only layer 1, increase the ratio, for example. A slightly smaller ratio is observed if a crosstalk constraint is imposed.

VII. CONCLUSION

In this paper, U3TLA-ILP3.0 which can consider layout constraints for three-layer bottleneck channel routing was proposed. For U3BCRP, U3TLA-ILP3.0 obtains a routing pattern which satisfies the layout constraints in a short time by using ILP and by restricting the layout patterns. A layout pattern obtained will be utilized as an initial solution to explore a detailed routing in bottleneck region with layout constraints efficiently.

Our future works include the extension of U3TLA-ILP3.0 to adopt more routing patterns and

TABLE I
COMPUTATION TIME

#nets	time [ms]	
	TLLL	3.0
12	596	8
18	141452	12
24	628764	13
30	>1h	13
60	>1h	21
150	>1h	89
*18	80327	11
*24	>1h	67

TABLE II
COMPUTATION TIME AND
FEASIBLE RATIO BY
U3TLA-ILP3.0

#nets	time [ms]	ratio [%]
60	20	98
150	78	100
300	279	100
600	1153	100
*60	43	94
*300	1087	98

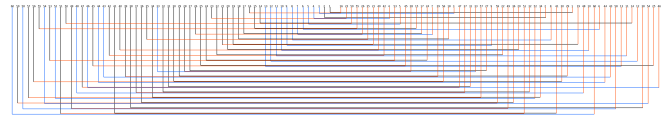


Fig. 13. A routing pattern obtained by using U3TLA-ILP3.0. #net= 60, (Agg, Vic)= ({37}, {15, 24, 41, 49, 58})

adapt it to the more general situations. For example, a pattern in which all three segments use the same layer can improve feasibility and reduce the number of vias. The formulation of U3TLA-ILP3.0 can be easily extended when more routing layers are available. It is challenging to be able to handle problems where pins are placed not only on upper boundaries.

REFERENCES

- [1] A.Kahng, J.Lienig, I.Markov, and J.Hu, “VLSI Physical Design: From Graph Partitioning to Timing Closure,” Springer, 2011.
- [2] A.Hashimoto and J.Stevens, “Wire Routing by Optimizing Channel Assignment within Large Apertures,” Proc. 8th Design Automation Workshop, pp.155-169, 1971.
- [3] T.Yoshimura and E.S.Kuh, “Efficient Algorithms for Channel Routing,” *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.CAD-1, No.1, pp.25-35, Jan.1982.
- [4] Y.Takashima, A.Takahashi, and Y.Kajitani, “Assignment of Intervals to Parallel Tracks with Minimum Total Cross-Talk,” *IEICE Trans. Fundamentals*, vol.E81-A, no.9, pp.1909-1915, 1998.
- [5] Y.Kajitani, “Order of Channels for Safe Routing and Optimal Compaction of Routing Area,” *IEEE Transactions on Computer-Aided Design*, Vol.CAD-2, No.4, pp.293-300, 1983.
- [6] W.M.Dai, T.Asano, and E.S.Kuh, “Routing Region Definition and Ordering Scheme for Building-Block Layout,” *IEEE Transactions on Computer-Aided Design*, Vol.CAD-4, No.3, pp.189-197, 1985.
- [7] D.F.Wong and C.L.Liu, “A New Algorithm for Floorplan Designs,” Proc. 23rd ACM/IEEE Design Automation Conference, No.1586075, pp.101-107, 1986.
- [8] K.Taniguchi, S.Tayu, A.Takahashi, Y.Todoroki, and M.Minami, “Bottleneck Channel Routing to Reduce the Area of Analog VLSI,” Proc. SASIMI 2022, pp.26-31, Hirosaki, Japan, October 2022.