Logic Gate Design Using Vertical Nanowire Transistors

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Abstract— Reducing power consumption of VLSI systems has become increasingly important. Although power consumption can be reduced by lowering the supply voltage, it is difficult to lower the supply voltage of conventional MOSFETs below 0.6V. In this study, we propose structure of logic gates using a novel device, VGAA-TFET (Vertical Gate-All-Around Tunnel Field-Effect Transistor), which is capable of operating at supply voltages lower than the minimum voltage limit of conventional MOSFETs and evaluate the proposed structures in terms of area and wire-length.

I. INTRODUCTION

Reducing the power consumption of VLSI systems is currently one of the most critical design constraints in energy-constrained embedded systems and high-performance, large-scale data centers. Although lowering supply voltage has a significant impact on power reduction, its reduction tends to saturate around 0.6 V [1]. To make a breakthrough, we have proposed a novel, emerging device called *VGAA-TFET (Vertical-Gate-All-Around Tunnel Field Effect Transistor)* [2] [3] [4]. The excellent switching characteristics of this device allow the supply voltage to be potentially reduced to about 0.1V, and the leakage current is extremely low, so a significant reduction in power consumption can be expected compared to existing CMOS circuits. Especially in terms of dynamic power consumption, a reduction of 98–99% is expected.

The next stage of this research is to explore higher level design space exploration, and the main questions are: 1) how to realize logic gates such as NOT and NAND gates by using such an emerging vertically-structured device, 2) how to estimate its efficiency in the logic gate level, and 3) analyze the impact and bottlenecks of VGAA-TFET-based functional blocks. To challenge these questions, this paper first proposes novel designs of vertically-structured VGAA-TFET-based logic gates and then introduces area and wire-length models for higher-level evaluation. Finally, by targeting a 1-bit full-adder circuit, we evaluate its function block level impacts. Although still the VGAA-TFET device technology is in an exploration phase, i.e., considering better materials, processes, etc., device-level and logic-gate-level co-design is a critical challenge for emerging device computing. As far as we know, this is the first trial to design VGAA-TFET-based logic functions, and we believe this is the starting point for nanowire-based ultra-low-power computing.

The paper is organized as follows. The structure and operating principle of VGAA-TFET are discribed in Section II. Section III shows the structure of logic gates using VGAA-TFETs, and Section IV outlines the area/wire-length modeling method. Section V presents evaluation results based on device parameter values that reflect both the current state and assuming future miniaturization. Finally, Section VI provides a summary and future issues.

II. VGAA-TFET

This section describes the structure and principle of operation of VGAA-TFETs.

A. VGAA-TFET Structure and Manufacturing Process

First, an overview of the VGAA-TFET manufacturing process is given. Fig. 1 shows a schematic of the nanowire growth process. A mask is formed on a thermally oxidized silicon substrate through lithography and etching, and nanowires are grown in selected areas on the silicon substrate by metalorganic vapor phase epitaxy (MOVPE) [5]. VGAA-TFET is then manufactured through the process shown in Fig. 2. BCB in Fig. 2 refers to benzocyclobutene resin, which acts as an insulation layer. Fig. 3 shows a cross-sectional structure of VGAA-TFET. VGAA-TFET has a vertical alignment of source electrode (light-green part) and drain electrode (orange part). The gate-all-around structure is formed by covering a portion of the nanowire (pink part) with gate oxide (blue part) and the gate electrode (yellow part).

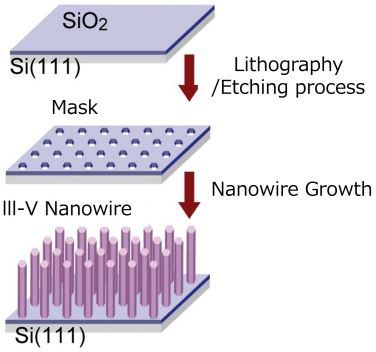


Fig. 1.Overview of Nanowire Growth[5]

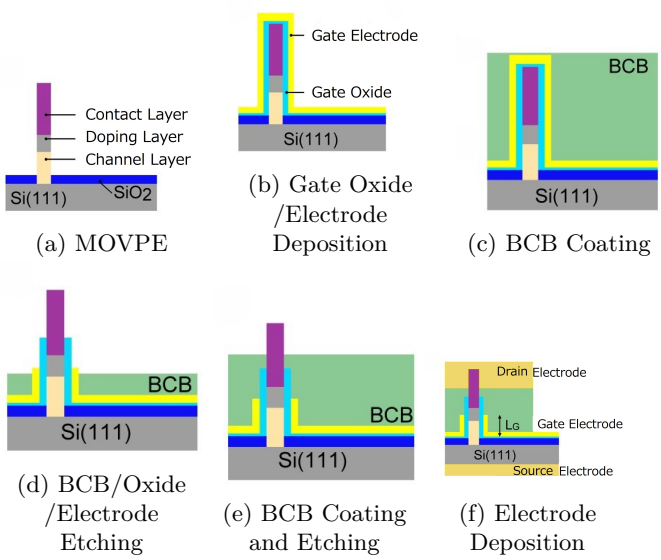


Fig. 2.VGAA-TFET Manufacturing Process[5]

B. How VGAA-TFET Works

The operation of a VGAA-TFET is similar to that of a general TFET (Tunnel Field Effect Transistor) and is based on the quantum tunneling effect. The quantum tunneling effect refers to the phenomenon in which electrons cross a potential barrier due to their wave nature. In VGAA-TFETs, electrons are ejected from the source side into the nanowire and become carriers due to the quantum tunneling effect. The VGAA-TFET shown in Fig. 3 operates as an n-type transistor, but it can be operated as a p-type transistor by reversing the voltage applied to the source/drain electrodes [6]. Hereafter, n-type VGAA-TFET and p-type VGAA-TFET are simply described as n-type and p-type transistors, respectively.

III. LOGIC GATES DESIGN USING VGAA-TFET

This section outlines the structure of logic gates using VGAA-TFETs.

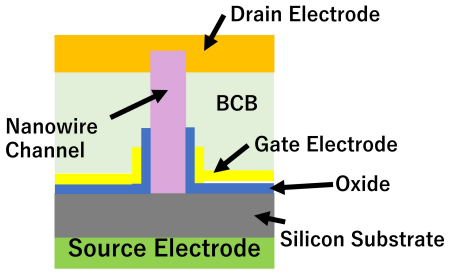


Fig. 3.VGAA-TFET Structure

A. NOT Gate

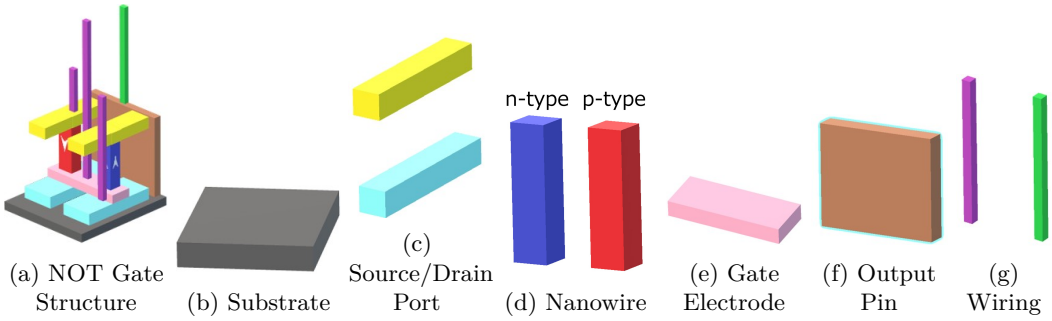
Fig. 4(a) shows the structure of a NOT gate using VGAA-TFETs. the NOT gate consists of the basic components shown in Fig. 4(b)- 4(g). First, Fig. 4(b) shows a silicon substrate. Nanowires (Fig. 4(d) are grown on this substrate . Red one is p-type and blue one is n-type. The bottom part of the nanowire is covered by the terminal (light blue) shown in Fig. 4(c). The carriers that jump into the nanowire due to the quantum tunneling effect are controlled by the voltage applied to the gate electrode shown in Fig. 4(e). The top of the nanowire is connected to the electrode (yellow) shown in Fig. 4(c); the light blue terminal is the drain side for p-type devices and the yellow electrode is the source side, and vice versa for n-type devices. Each drain is connected to the output pin in Fig. 4(f). The inputs to the gate and each terminal and the outputs from the output pins are propagated through the wiring shown in Fig. 4(g).

B. 2-Input NAND Gate

Fig. 5 shows the structure of a NAND gate. The difference between NAND gate and NOT gate is that two p-type transistors are connected in parallel and two n-type transistors are connected in series, as in an ordinary CMOS circuit. First, the parallel connection method is described. Focus on the p-type (red) VGAA-TFET in Fig. 5(a), the two p-type VGAA-TFETs are connected at both the drain terminal (lower light blue terminal) and the source terminal (upper yellow terminal). This enables parallel connection.Next, we focus on the n-type (blue) VGAA-TFETs in Fig. 5(a).These two VGAA-TFETs are connected by combining the drain terminal (upper yellow terminal) of one VGAA-TFET(N1) to the source terminal (lower light blue terminal) of the other VGAA-TFET(N2). This enables a series connection. Various circuits can be configured by using the parallel and series connection methods described above.

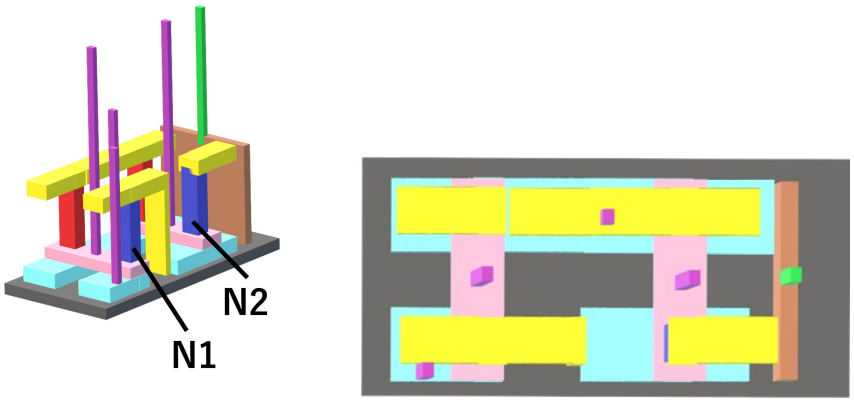
C. 2-Input XOR Gate

Fig. 6 shows the structure of a XOR gate. In Fig. 6(a), on the p-type transistor side above the output line, two series structures consisting of two p-type transistors are



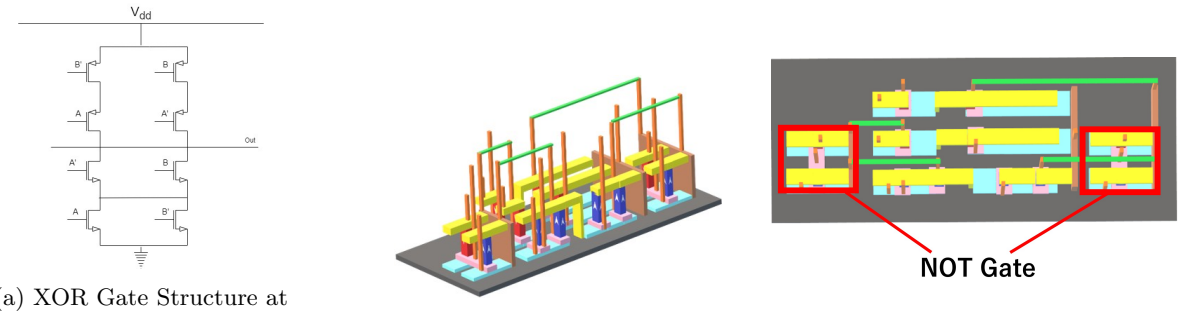
(a) NOT Gate Structure (b) Substrate (c) Source/Drain Port (d) Nanowire (e) Gate Electrode (f) Output Pin (g) Wiring

Fig. 4.NOT Gate and Basic Components of Logic Gate



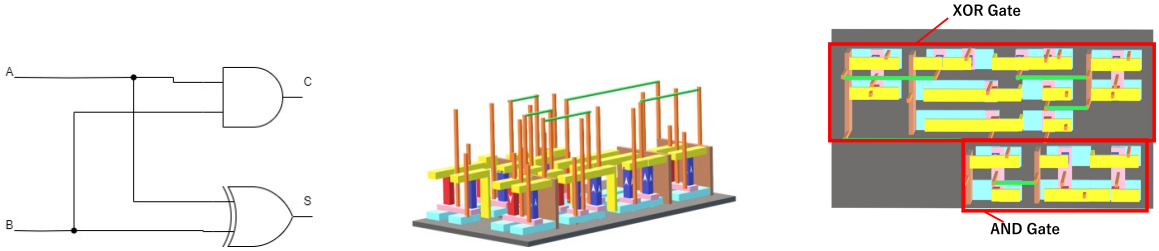
(a) NAND Gate 3D Structure (b) NAND Gate Footprint

Fig. 5.NAND Gate Structure



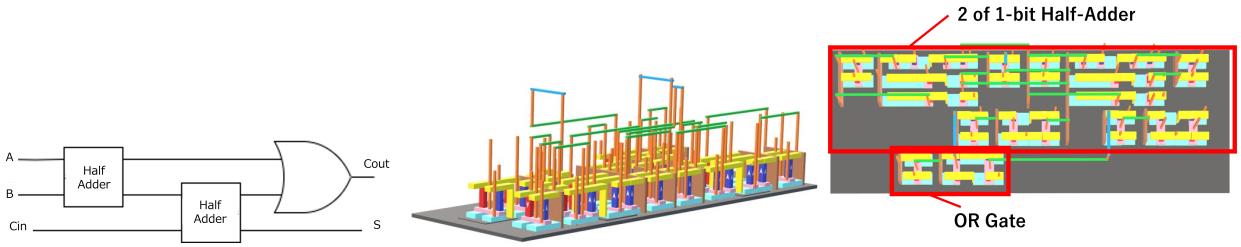
(a) XOR Gate Structure at Transistor Level (b) XOR Gate 3D Structure (c) XOR Gate Footprint

Fig. 6.XOR Gate Structure



(a) 1-bit Half-Adder at Gate Level (b) 1-bit Half-Adder 3D Structure (c) 1-bit Half-Adder Footprint

Fig. 7.1-bit Half-Adder Structure



(a) 1-bit Full-Adder at Gate Level (b) 1-bit Full-Adder 3D Structure (c) 1-bit Full-Adder Footprint

Fig. 8.1-bit Full-Adder Structure

connected in parallel at the output. On the other hand, on the n-type transistor side below the output line, two sets of parallel structures consisting of two n-type transistors are connected in series. To realize this structure using VGAA-TFET, the parallel/series structure construction method described in Section III.B was applied. In Fig. 6(a), A' and B' represent the negation of inputs A and B respectively, and thus two NOT gates are included in a XOR gate(Fig. 6(c)).

D. 1-bit Half-Adder

Fig. 7 shows the structure of a 1-bit half-adder. The half-adder consists of an AND gate and an XOR gate; the AND gate is a combination of the NOT and NAND gates shown in Section III.A and III.B and is located at the bottom of Fig. 7(c). On the other hand, the XOR gate is located on the upper side of the figure. The light-green wiring represents the wiring between the gates.

E. 1-bit Full-Adder

Fig. 8 shows the structure of a 1-bit full-adder. The full-adder is composed of two 1-bit half-adder and an OR gate. In Fig. 8(c), the two 1-bit half-adders are located on the upper side. The OR gate, consisting of a NOR gate and a NOT gate, is located below the half-adder.

IV. BASIC LOGIC GATE AREA/WIRE-LENGTH MODELING

This section describes area/total wire-length/longest wire-length modeling for logic gates using VGAA-TFETS.

A. Area Modeling

The modeling of area and wire-length is achieved using the parameters shown in Table I. From Fig. 9, the area can be approximated as follows where S_{NAND} is the area of the NAND gate, L_{NAND} is the vertical length of the NAND gate, W_{NAND} is the horizontal length of the NAND gate.

$$S_{NAND} = L_{NAND} \times W_{NAND} \quad (1)$$

$$W_{NAND} = 2W_s + W \quad (2)$$

$$L_{NAND} = L_o + L_1 + L_2 + 2L_n + X \quad (3)$$

Thus, the product of the vertical length L_{NAND} and the horizontal length W_{NAND} of the NAND gate gives the area. The same method can be used to model the area of the NOT gate shown in Section III. Table II shows area models for logic gates other than NAND gates.

B. Wire-Length Modeling

The wire-length refers to the length of the path that the carriers pass through when the VGAA-TFET is on. Fig. 10 shows an example of paths in a NAND gate. In this case, green part indicates the total path that carriers pass through when the VGAA-TFETs that make up the circuit are turned on, and red arrows indicate the paths that the ejected carriers pass through on each type of VGAA-TFETs. First, the total wire-length is explained. The total wire-length is the sum of the p-type and n-type wire-lengths. When the VGAA-TFETs that make up the circuit are turned on, current flows and charge is accumulated. The accumulation of charge results in power consumption due to parasitic capacitance and wiring capacitance. The total wire-length is proportional to the parasitic capacitance and wiring capacitance of the circuit, which is also proportional to the power consumption. In the case of Fig. 10, the total wire-length is the sum of the p-type and n-type wire-lengths, so the equation is expressed as (4). Next, the longest wire-length is explained. The longest wire-length is the path that has the greatest length of all the paths that make up the circuit. It is considered to be mainly proportional to the delay of the circuit, since it means the longest path that the carriers pass through in the circuit. In the case of Fig. 10, the longest path is the red arrow in Fig. 10(a), and this is expressed as (5).

$$\text{Total Wire Length} = 5H + 2L_2 + L_n + X + Y \quad (4)$$

$$\text{Longest Wire Length} = 3H + Y + L_n + L_2 \quad (5)$$

The same method can be used to model wire-lengths for NOT and NOR gates. Table II shows models of total wire-length and longest wire-length of basic logic gates.

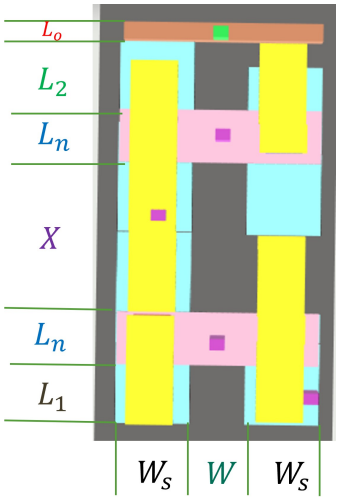


Fig. 9.Parameters Used for Area Modeling

TABLE I
Parameters

Name	Meaning	Assuming Future Process Data[nm]	Current Data[nm]
X	distance between NWs	400	2000
Y	vertical distance in series connection	400	1000
L_n	NW's vertical length	25	200
L_o	vertical length of output pin	300	1000
L_1	distance to the first NW	400	2000
L_2	distance between the last NW and output pin	300	500
W	distance between silicon wires	300	500
W_s	silicon wire width	300	1000
H	NW length	1000	1000

V. EVALUATION

To estimate the impact of VGAA-TFET on the area/power consumption/delay of the considered circuits, the area, total wire-length, and longest wire-length of the 1-bit full-adder were evaluated. The model presented in Section IV and the process data values shown in Table I were used. The 1-bit full-adder consists of multiple logic gates as described in Section III.E.In this evaluation, as an initial study, we discuss the lower limit performance ignoring the wire-length and area between logic gates. In Table I, the "Current Data" refers to measured data obtained from current device-level experiments. On the other hand, the "Assuming Future Process Data" represents projected values assuming future scaling, based on the minimum resolution of photolithography in the manufacturing process. To evaluate the future scalability of circuits using VGAA-TFETs, as well as the impact of such scaling on circuit area, power consumption, and delay, the evaluation was conducted using both types of data.

Fig. 11 shows the evaluation results for area, total wire-length, and longest wire-length, respectively. The "Current" is the result using the current process data, and the "Assuming Future Process" is the result using the data assuming future process. First, comparing the "Currrent" and "Assuming Future Process" in Fig. 11(a) shows that the area can be reduced to about one-tenth by miniaturization, and Fig. 11(b) and Fig. 11(c) show that both the total wire-length and longest wire-length can be reduced

TABLE II
Area/Total Wire-Length/Longest Wire-Length Models of Basic Logic Gates

Logic Gate	Area	Total Wire-Length	Longest Wire-Length
NOT Gate	$(2W_s+W)\times(L_n+L_o+L_1+L_2)$	$2H+2L_2$	$H+L_2$
NOR Gate	$(2W_s+W)\times(L_o+L_1+L_2+2L_n+X)$	$5H+2L_2+L_n+X+Y$	$3H+Y+L_n+L_2$
XOR Gate	$(3W_s+2W)\times(3L_1+3L_2+3L_o+6L_n+2X+Y)$	$13H+7L_2+7L_n+6X+3Y$	$H+L_2+3H+2X+Y+2L_n+L_2$

to about half. Next, a comparison is made between the percentage occupied by VGAA-TFET and the percentage occupied by the peripheral elements in each item. The red portion of the graph in Fig. 11 shows the percentage of VGAA-TFET, and the light-green portion shows the percentage of peripheral elements. Fig. 11(a) shows that the peripheral elements currently account for 96.9% of the total area, and this percentage will increase as miniaturization progresses. Fig. 11(b) shows that the peripheral elements account for 64.8% of the total wire-length, and Fig. 11(c) shows that the peripheral elements account for 61.5% of the longest wire-length. The above results indicate that the peripheral elements have a significant impact on circuits using VGAA-TFETs.

VI. CONCLUSION

In this paper, we proposed the structure of circuits using VGAA-TFETs composed of nanowires as a new device, and evaluate the future miniaturization of circuits and changes in the impact of VGAA-TFETs due to miniaturization. The circuit structures are shown from basic logic gates such as NOT and NAND gates to a 1-bit full-adder. The evaluation results of the area, total wire-length, and longest wire-length of the 1-bit full-adder were reported. From the evaluation results, it was found that the influence of peripheral elements on circuits using VGAA-TFETs is significant. The logic gate structure reported in this paper is an initial study, and there is still room for reducing the area and wire-length. In addition, the actual power consumption and circuit delay have not yet been evaluated. Therefore, we will optimize the circuit structure and model the power consumption and delay of the circuit based on the results of this study.

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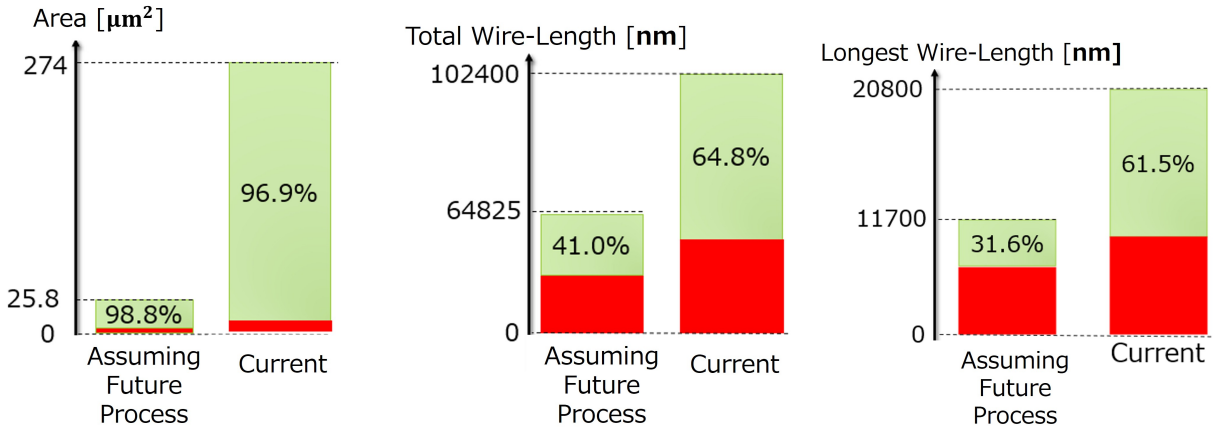
(a) Wire-Length of n-type Side (b) Wire-Length of p-type Side

Fig. 10.Wire-Length of NAND Gate



(a) Area (b) Total Wire-Length (c) Longest Wire-Length

Fig. 11.Evaluation Results of Area/Total Wire-Length/Longest Wire-Length
(Red:VGAA-TFET Light Green:Peripheral Elements)

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