# Comparison of latch-based circuit and flip-flop-based circuit in actual device

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**Abstract - This paper reports the comparison results of current consumption, maximum operating frequency characteristics (Fmax), and minimum operating voltage characteristics (Vmin) of latch-based and flip-flop-based circuits. The latch-based circuits, under certain conditions, consume less current, have a higher Fmax at the same voltage, and a lower Vmin at the same frequency. These results show that latch-based circuits can reduce power at the same frequency as flip-flop-based circuits.**

## I. Introduction

### *A. Background*

Flip-flop-based circuits using flip-flops are used as synchronous logic circuits. On the other hand, the superiority of latch-based circuits using latches over flip-flop-based circuits in low power and high-speed operation characteristics is often discussed [1-7]. Previous studies [2,5, 7] in which comparative evaluation results with EDA tools are described have been reported, but there are no previous studies in which comparison results with actual devices are reported. In literature [8], an example of specification derivation of an evaluation chip is introduced, and evaluation results with EDA tools are shown, but results with actual devices are not shown. This paper reports the comparison results of current consumption, Fmax characteristics, and Vmin characteristics of an evaluation chip made based on the example specifications described in literature [8].

### *B. Structure of this paper*

In section 2, the analysis/confirmation items, their measurement conditions, and the four layers of the test pattern introduced in literature [8] are explained, and section 3 shows the analysis and evaluation results of current consumption. The comparison results of current consumption between EDA and actual devices are described, and the difference of current consumption between latch-based circuit and flip-flop-based circuit, frequency dependence, and temperature dependence in the test pattern stratification are described. Section 4 shows the analysis and evaluation results of Fmax and Vmin characteristics. The confirmation results of the Shmoo plot are described, and the difference of Fmax and Vmin between latch-based circuit and flip-flop-based circuit are described. Section 5 summarizes this paper.

## II. Analysis/Confirmation Items and Measurement Conditions

This section outlines the analysis and confirmation items, along with their measurement conditions, and explains a detailed description of the 4 layers of the test pattern introduced in literature [8]. Table 1 shows the analysis/ confirmation items and their measurement conditions. The test pattern consists of the following 4 layers described in literature [8]. These layers, in ascending numerical order, have higher circuit activation rates and consume higher power in EDA.

I. All input 24 bits are fixed constant (Hereinafter, this test pattern is called Const.)
II. The upper 12 bits are fixed constant, the lower 12 bits from 1 bit to 12 bits are random number input, and the rest are fixed constant (Hereinafter, this test pattern is called Upper Random.)
III. The lower 12 bits are fixed constant, the upper 12 bits from 1 bit to 12 bits are random number input, and the rest are fixed constant (Hereinafter, this test pattern is called Lower Random.)
IV. 24 bits from 13 bits to 24 bits are random number input, and the rest are fixed constant (Hereinafter, this test pattern is called All Random.)

For each layer, 15 test patterns (P00 to P14) were created in the order of increasing the power consumption evaluation value of the flip-flop base circuit in EDA. There are 12 measurement frequencies (A to K). There are 3 measurement temperatures (low, room, and high), which are referred to as LT/RT/HT. There are 3 measurement voltages (Low, Typical, and High), which are referred to as LV/TV/HV. There are 3 types of wafers (Typical, Worst, and Best), which are referred to as TT/SS/FF wafers. In the measurement of the current consumption, 12 chips are measured for each wafer, and chips that fail by function confirmation are excluded in the analysis.

In the measurement of the frequency dependence and temperature dependence of the current consumption, 3 chips are measured for each wafer, and function pass/fail is ignored. In the measurement of the shmoo plot, 1 chip is measured for each wafer, and the function pass position when frequency and voltage are swung is measured. The trend was confirmed from the measurement results, and the analysis/confirmation was conducted by narrowing down the conditions. In the next section, the analysis/confirmation results are described. In this paper, not all results are extracted, and the results are described as relative values with the maximum or minimum value set to 1.

TABLE I
Analysis/confirmation items and measurement conditions

| Analysis/confirmation items | Measurement conditions | | | | | |
|---|---|---|---|---|---|---|
| | Test patterns | Frequency | Temperature | Voltage | Wafer | Number of chips |
| Current consumption | 60 patterns(4×15) Const/UpperRandom/LowerRandom/AllRandom, P00-P14 | C/D/E | LT RT HT | LV TV HV | SS TT FF | 12 |
| Frequency dependence and temperature dependence of current consumption | 60 patterns(4×15) Const/UpperRandom/LowerRandom/AllRandom, P00-P14 | A/B/C/D/E/F/G/H/I/J/K/L | LT RT HT | TV | SS TT FF | 3 |
| Shmoo Plot | 12 patterns(4×3) Const/UpperRandom/LowerRandom/AllRandom, P01/P07/P13 | Frequency Swing | LT RT HT | Voltage swing | SS TT FF | 1 |
| Fmax characteristics | | D/G | | Voltage swing | | |
| Vmin characteristics | | Frequency Swing | | LV TV | | |

## III. Analysis/evaluation results of current consumption

This section presents the analysis and evaluation results of current consumption. It details the comparison of current consumption between EDA results and actual devices, as well as the differences in current consumption between latch-based and flip-flop-based circuits. Additionally, the frequency dependence and temperature dependence observed in the test pattern for each layer are discussed.

### *A. Confirmation of current consumption*

The EDA evaluation results and actual device measurement results of the current consumption of the flip-flop base circuit and the latch base circuit are shown in Fig. 1. On the horizontal axis of the figure, 60 test patterns are arranged in order of the increase in the EDA power consumption of the flip-flop base circuit. From the figure, the EDA evaluation results show that the latch base circuit consumes less current than the flip-flop base circuit in all test patterns. On the other hand, the actual device measurement results show that the latch base circuit consumes more current than the flip-flop base circuit in the test pattern with low EDA power consumption (left side of the dotted line in Fig. 1 (b)). In the test pattern with high EDA power consumption (right side of the dotted line in Fig. 1 (b)), the latch base circuit consumes less current than the flip-flop base circuit. These results confirm that the actual device measurement results are different from the EDA evaluation results.

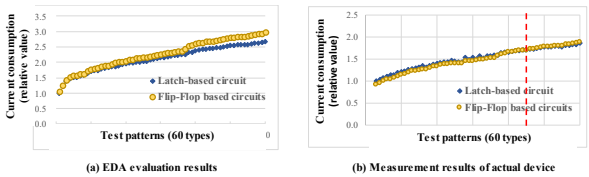



Fig. 1. EDA evaluation results and actual device measurement results of current consumption (relative value) (Frequency: D, Temperature: RT, Voltage: TV, Wafer: TT)

### *B. Confirmation of current consumption difference by layer*

Figures 2 to 4 show the measurement results of actual devices divided by layer regarding current consumption difference (current consumption of flip-flop-based circuit – current consumption of latch-based circuit). From Figs. 2, 3, and 4, it was confirmed that the difference in current consumption was negative (the current consumption of the latch base circuit was large) in all test patterns from P00 to P14 in the case of Const and Upper Random. On the other hand, in the case of Lower Random and All Random in Figs. 3 and 4, it was confirmed that the difference in current consumption was positive (the current consumption of the latch base circuit was small) in the test pattern with large EDA power consumption (red shaded area in Figs. 3 and 4).

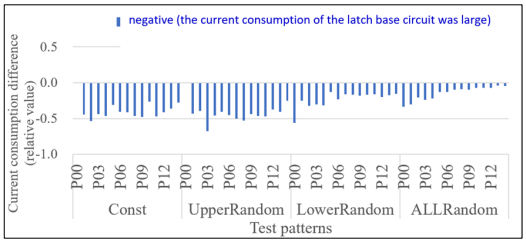



Fig. 2. Current Consumption difference results by layer (relative value) (Frequency: C, Temperature: LT, Voltage: LV, Wafer: SS)

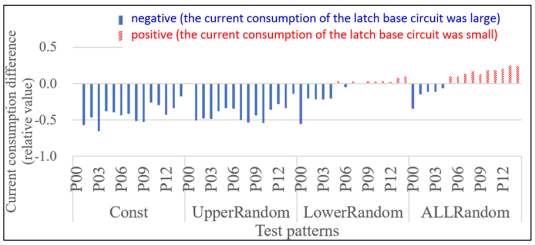



Fig. 3. Current consumption difference results by layer (relative value) (Frequency: D, Temperature: RT, Voltage: TV, Wafer: TT)

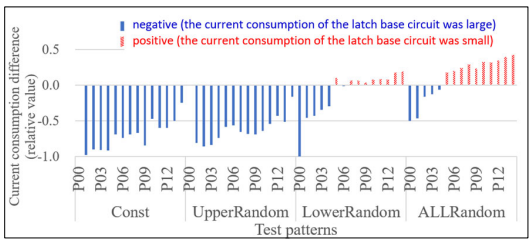
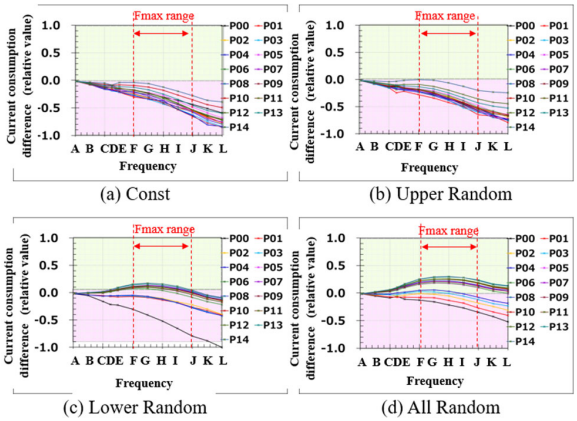



Fig.4. Current consumption difference results by layer (relative value) (Frequency: E, Temperature: HT, Voltage: HV, Wafer: FF)

### C. *Confirmation of frequency dependence of current consumption difference*

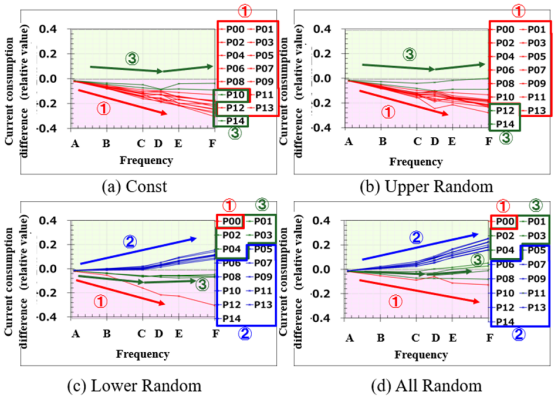
The frequency dependence of current consumption difference (current consumption of flip-flop base circuit – current consumption of latch base circuit) is described. In the frequency dependence, three trends were confirmed. For example, the measurement results of temperature: HT, voltage: TV, and wafer: SS are shown in Figs. 5 and 6. Fig. 5 shows the measurement results up to frequency L, where the Fmax of each evaluation chip falls within the range of F to L. Consequently, when the frequency is below F, all evaluation chips operate within their designated range. Fig. 6 is an enlarged diagram up to frequency F to clarify the trend up to Fmax. The first trend is that for the test pattern with low EDA power consumption ((1) red arrow in Fig. 6), the difference in current consumption is negative (the current consumption of the latch base circuit is large) and tends to fall to the right with respect to frequency. The second trend is that for the test pattern with high EDA power consumption ((2) blue arrow in Fig. 6), the difference in current consumption is positive (the current consumption of the latch base circuit is small) and tends to rise to the right with respect to frequency. The third trend is that for the test pattern with intermediate EDA power consumption ((3) green arrow in Fig. 6), the difference in current consumption is negative (the current consumption of the latch base circuit is large) at low frequency. However, as the frequency increases, the difference in current consumption becomes small and, in some cases, becomes positive (the current consumption of the latch base circuit is small). From the second and third trends, it is considered that the effect of suppressing the current consumption of the latch increases as the test pattern and frequency increase and the current consumption increases.



(a) Const (b) Upper Random

(c) Lower Random (d) All Random

Fig.5. Frequency Dependence Results of the current consumption difference (relative value) (Frequency: A-L, Temperature: HT, Voltage: TV, Wafer: SS)



(a) Const (b) Upper Random

(c) Lower Random (d) All Random

Fig.6. Frequency dependence of current consumption difference (relative value) Enlarged to F (Frequency: A-F, Temperature: HT, Voltage: TV, Wafer: SS)

### D. *Confirmation of temperature dependence of current consumption difference*

Temperature dependence of current consumption difference (current consumption of flip-flop base circuit – current consumption of latch base circuit) is shown in Table 2. Figs. 7 to 10 show temperature dependence of current consumption difference at frequencies A (low frequency), D (intermediate frequency), F (high frequency 1), and L (high frequency 2) of wafer TT. From Table 2 and Fig. 10, the current consumption difference goes up to the right in the frequency band near Fmax beyond G for all wafers, and the current consumption difference tends to increase as the temperature increases. Therefore, in the frequency band near Fmax, the higher the temperature, the greater the current consumption suppression effect of the latch.

TABLE II
Temperature dependence of current consumption difference

| Wafer | Frequency | Temperature Dependent Results |
|---|---|---|
| SS | A,B (low) | No characteristics are observed with respect to temperature. |
| | C,D (intermediate) | For EDA test patterns that consume a lot of power, the difference in current consumption increases with temperature. |
| | E～L (high) | The difference in current consumption increases with temperature. |
| TT | A (low) | The difference in current consumption decreases with temperature. |
| | B~E (intermediate) | No characteristics are observed with respect to temperature. |
| | F (high-1) | For EDA test patterns that consume a lot of power, the difference in current consumption increases with temperature. |
| | G~L (high-2) | The difference in current consumption increases with temperature. |
| FF | A (low) | The difference in current consumption decreases with temperature. |
| | B～F (intermediate) | No characteristics are observed with respect to temperature. |
| | G~K (high) | For EDA test patterns that consume a lot of power, the difference in current consumption increases with temperature. |
| | L | Not measured (cannot be measured due to overcurrent at HT) |

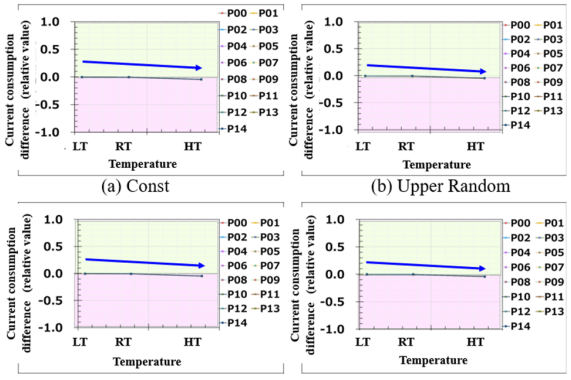
### E. *Summary of current consumption*

From the measurement results of current consumption of the evaluation chip, it was confirmed that the latch-based circuit consumed more current than the flip-flop-based circuit in the test pattern with low EDA power consumption. On the other

hand, it was confirmed that the latch-based circuit consumed less current than the flip-flop-based circuit in the test pattern with high EDA power consumption, high frequency region, and high temperature. From these results, it was confirmed that the latch-based circuit can reduce the power consumption when the current consumption is large. It was proven that the latch-based circuit can reduce the power consumption. It was confirmed that the actual device measurement result was different from the EDA evaluation result. However, consideration of this factor is not discussed and only the result is described because it is beyond the scope of this research report.

## IV. Analysis and evaluation results of Fmax and Vmin characteristics

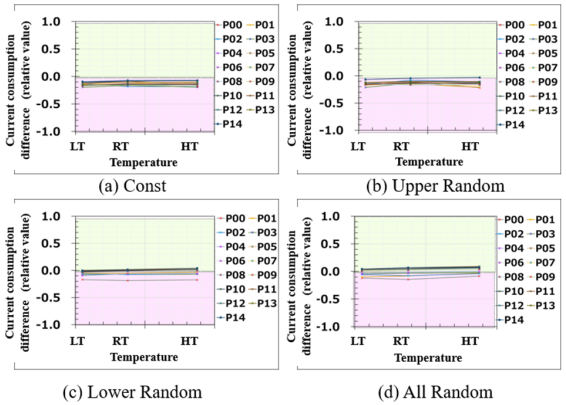
This section presents the analysis and evaluation results of Fmax and Vmin characteristics. The confirmation results of the Shmoo plot are discussed, along with the differences in Fmax and Vmin between the latch-based circuit and the flip-flop-based circuit.




(a) Const (b) Upper Random

(c) Lower Random (d) All Random

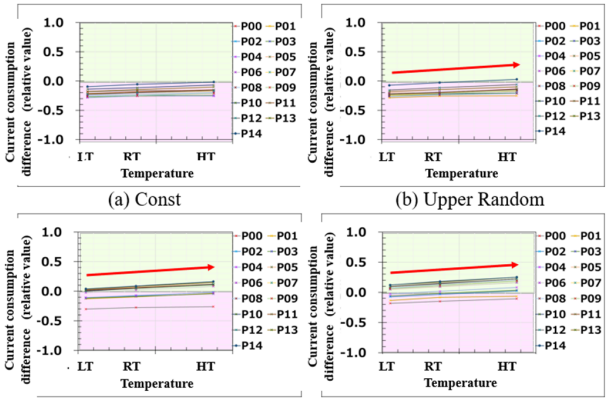
Fig.7.Temperature dependence of current consumption difference (relative value) (Frequency: A, Temperature: LT, RT, HT, Voltage: TV, Wafer: TT)




(a) Const (b) Upper Random

(c) Lower Random (d) All Random

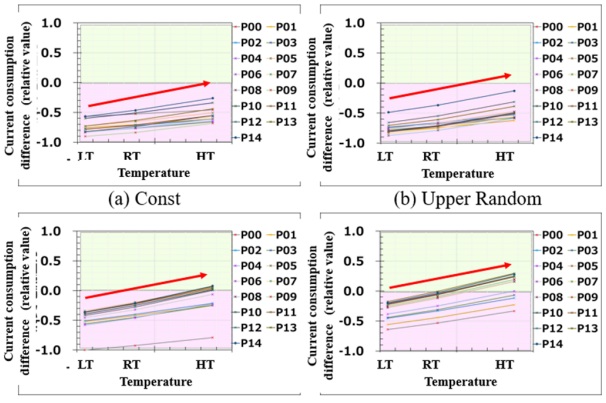
Fig.8.Temperature dependence of current consumption difference (relative value) (Frequency: D, Temperature: LT, RT, HT, Voltage: TV, Wafer: TT)




(a) Const (b) Upper Random

(c) Lower Random (d) All Random

Fig.9.Temperature dependence of difference in current consumption (relative value) (Frequency: F, Temperature: LT, RT, HT, Voltage: TV, Wafer: TT)




(a) Const (b) Upper Random

(c) Lower Random (d) All Random

Fig.10.Temperature dependence of difference in current consumption (relative value) (Frequency: L, Temperature: LT, RT, HT, Voltage: TV, Wafer: TT)

### *A. Confirmation of the Shmoo plot*

Figures 11 to 13 show the period vs voltage Shmoo plot. In the figure, the results of the flip-flop-based circuit and the latch-based circuit are superimposed. Dark blue is the measurement result of the flip-flop-based circuit, and red is the measurement result of the latch-based circuit. Dark blue and red represent the function pass, and white represents the function fail. From the figure, the shape of the shmoo plot shows the bipolar characteristic, and the cause of the function fail is a setup constraint violation inside the circuit. It is also found that the latch-based circuit tends to have better Fmax and Vmin characteristics than the flip-flop-based circuit overall. However, it is also confirmed that the flip-flop-based circuit tends to have better Fmax characteristics than the latch-based circuit, as shown in the high voltage and high frequency side of the Upper Random P13 (framed in Figures 11,12 and 13).

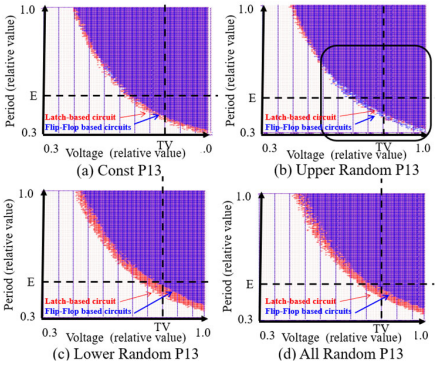



Fig.11.Period vs. voltage Shmoo plot (relative value) (Temperature: LT, Wafer: TT)

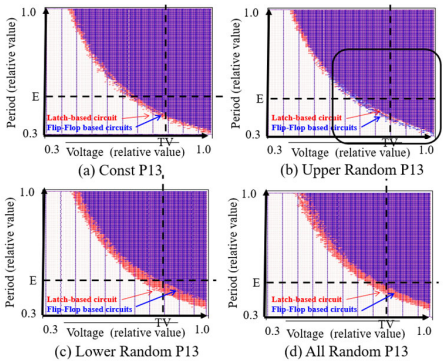



Fig.12. Period vs. voltage Shmoo plot (relative value) (Temperature: RT, Wafer: TT)

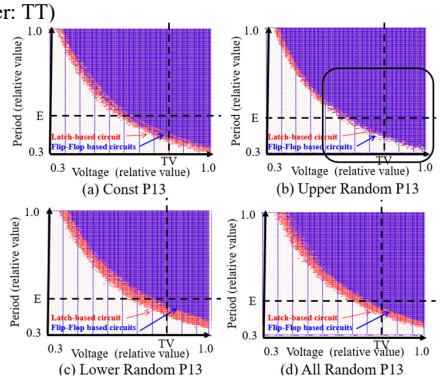



Fig.13.Period vs. voltage Shmoo plot (relative value) (Temperature: HT, Wafer: TT)

## B. *Fmax difference check*

Figure 14 shows an example of measurement results of Fmax difference (Fmax of flip-flop base circuit - Fmax of latch base circuit). As shown in Figure 14, it was confirmed that Fmax difference becomes negative (Fmax of latch base circuit is high) under many conditions. However, it was also confirmed that Fmax difference becomes positive (Fmax of latch base circuit is low) such as Const P01 at temperature LT and Upper Random P13 at temperature HT (red shaded area in Figure 14). This is the same as the tendency on the high voltage side of Upper Random P13 observed in the confirmation of the shmoo plot.

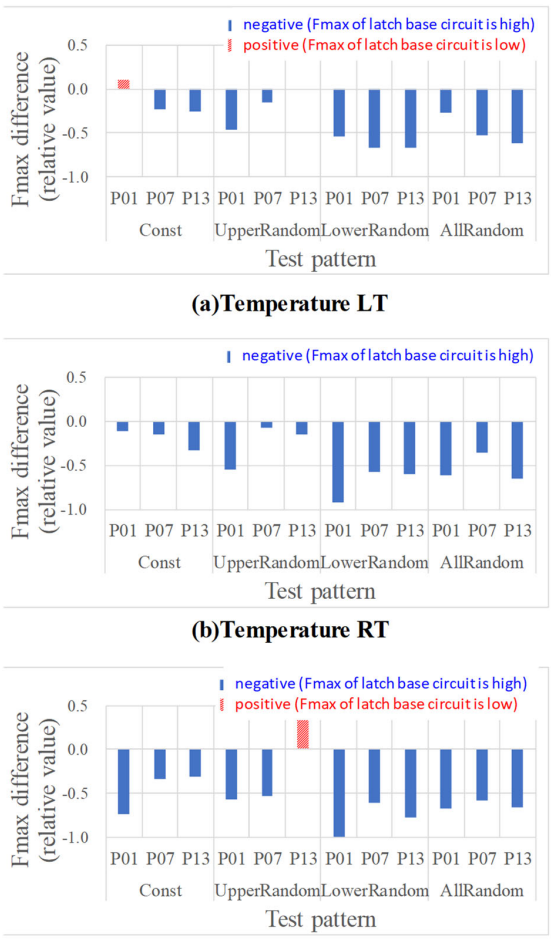



Fig.14. Fmax difference measurement result (relative value) (Voltage: TV, Wafer: TT)

## C. *Vmin difference confirmation*

Figure 15 shows an example of the measurement result of Vmin difference (Vmin of flip-flop base circuit - Vmin of latch base circuit). From the figure, it was confirmed that Vmin difference was positive (Vmin of latch base circuit was small). However, it was also confirmed that Vmin difference was negative (Vmin of latch base circuit was large) as in Upper Random P13 (red shaded area in Figure 15). This is the same tendency on the high frequency side of Upper Random P13 as seen in the confirmation of the shmoo plot.

## D. *Summary of Fmax and Vmin characteristics*

From the confirmation results of the shmoo plot, Fmax difference, and Vmin difference, it was confirmed that the latch base circuit had better Fmax and Vmin characteristics than the flip flop base circuit. However, like the Upper Random P13, the characteristics are different, and the flip-flop base circuit has good Fmax and Vmin characteristics.

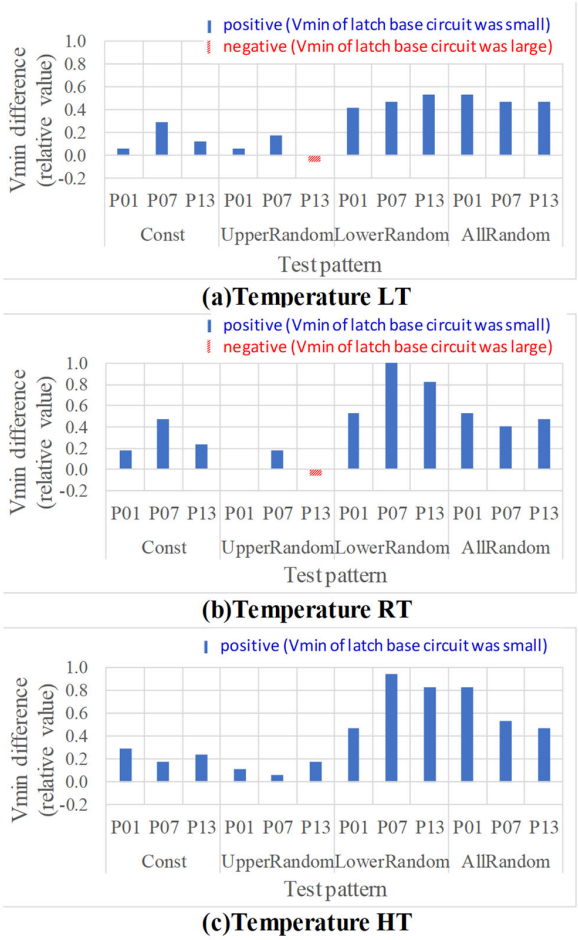



Fig.15.Measurement result of Vmin difference (relative value) (Frequency: E, Wafer: TT)

This may be due to the evaluation circuit structure and test pattern characteristics. As shown in Figure 5 of Reference [8], the evaluation circuit structure is an arithmetic circuit that actively incorporates a reconvergence structure, and the critical path is a path from the lower bit input to the upper bit output. Upper Random has a pattern characteristic that tends to become a structure in which the path from the lower bit input to the upper bit output is activated, since the upper bit input is fixed, and the lower bit input is changed. If All Random changes the lower bit input but also the upper bit, and the path from the lower bit input and the path from the upper bit input collide with the path from the upper bit input by AND, the possibility that the input from the upper bit input to AND becomes 0 is higher than that of the constant input by changing the upper bit input, and the path from the lower bit input is suppressed, and there is no critical path from the lower bit input to the upper bit output. Therefore, the Upper Random pattern is the most likely to activate the critical path. From the confirmation result of the Shmoo plot, the rate-limiting cause of Fmax is the violation of the setup constraint in the circuit. It is thought that distinctive characteristics are likely to be observed in Upper Random where the critical path is easily activated.

## V. Conclusion

Comparison of current consumption, maximum operating frequency (Fmax) characteristics and minimum operating voltage (Vmin) characteristics of latch-based circuit and flip-flop-based circuit was conducted. The following results were obtained. Regarding current consumption, latch-based circuit consumed more current than flip-flop-based circuit in test pattern with low EDA power consumption. On the other hand, latch-based circuit consumed less current than flip-flop-based circuit in test pattern with high EDA power consumption, high frequency region, and high temperature. Therefore, when current consumption is large. It was found that latch-based circuit can reduce power consumption. It was confirmed that actual device measurement result was different from EDA evaluation result. However, consideration of this factor is not discussed and only the result is described. Regarding Fmax and Vmin characteristics, Fmax was high at the same voltage and Vmin was low at the same frequency. It was found that latch-based circuit can reduce power consumption at the same frequency compared with flip-flop-based circuit.

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