Voltage and Frequency Dependence of Single Event Transient Induced by Alpha-Particle

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Abstract— A soft error on a semiconductor chip is a temporary malfunction in a latch or flip-flop (FF). Soft errors caused by Single Event Transients (SETs) become more significant at high clock frequencies over GHz. This study investigated the frequency dependence of SETs using a test circuit that eliminates the influence of Single Event Upsets (SEUs). By irradiating the circuit with alpha particles while the clock was running, soft error rates (SERs) were measured. A linear increase in SERs was observed below 700 MHz.

I. Introduction

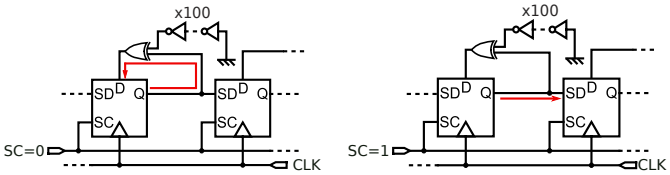
In recent years, the miniaturization of transistors decreases reliability[1]. One of the factors is the soft errors. Soft errors occur when a radiation particle strikes a transistor on an integrated circuit, flipping a stored value of a latch or flip-flop (FF). Soft errors are categorized as Single Event Upsets (SEUs) in storage elements and Single Event Transients (SETs) in combinational circuits. SET-induced errors increase with operating frequency due to more frequent latching frequencies[2]. Therefore, accurate evaluation of the frequency dependence of SETs is essential for designing resilient systems. In addition, as circuits increasingly operate at lower supply voltages for low power, SET pulse widths become wide, increasing the probability of being latched. Thus, supply voltage is also a critical factor affecting soft error susceptibility.

However, most existing dynamic test circuits cannot separate SETs from SEUs, limiting accurate evaluation[3]. This paper proposes a circuit that enables high resolution measurement of SETs as a function of clock frequency without influence from SEUs. Using this circuit, we conducted alpha-particle irradiation experiments, which is one of the dominant radiation sources in terrestrial environments. The proposed method enabled a clear evaluation of the frequency and supply voltage dependence of soft error behavior under terrestrial conditions.

II. Proposed Method

A. *Dynamic soft error test circuit with SEU Tolerant FFs*

During dynamic soft error tests, the clock signal(CLK) must be continuously applied. One of conventional soft error tests is to cascade FFs. However, captured errors in FFs disappear. Therefore, it is mandatory to construct a circuit that can store captured errors while applying CLK. Previous studies have proposed dynamic soft error testing using SCANFFs[3]. Fig. 1 shows operation of the circuits. In the SCANFF, the inputs port is switched by the control signal SC. When SC=0, the output port is looped back to the input (D = Q) to hold the error. When SC = 1, the output is transferred to the next stage to perform readout.



(a)SC=0(Measurement mode) (b)SC=1(Readout mode)

Fig. 1. Operation of the dynamic measurement circuit using SCAN flip-flops

To accurately evaluate SETs without SEUs, we adopted a SCANFF based on a Dual Interlocked Cell (DICE) structure, which is known for its strong SEU tolerance.

B. *Multi Frequency Parallel Evaluation*

Fig. 2 shows the schematic of the proposed circuit to evaluate SETs at multiple operating frequencies. In this design, 2.56 GHz, 3.2 GHz, and 4.0 GHz clocks are generated from a ring oscillator, and one of them is selected as the input. The selected clock is then divided by 1/2, 1/4, ..., up to 1/128 using frequency dividers and distributed to seven FF blocks, thereby avoiding excessive power consumption due to high-frequency operation across all FFs. Each block contains 784-stage SCANDICEFFs, with clock signals distributed via a buffer chain to 112 FFs per multiplexer segment.

III. Alpha-particle irradiation

A test chip was fabricated in a 65 nm bulk CMOS process. The soft error tolerance of the proposed circuit was evaluated under alpha-particle irradiation, which is one of the dominant sources of soft errors in terrestrial environ-

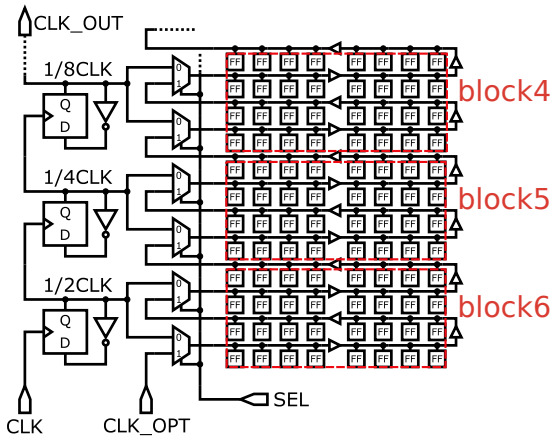


Fig. 2. A dynamic test circuit that enables soft error evaluation under multiple clock frequencies

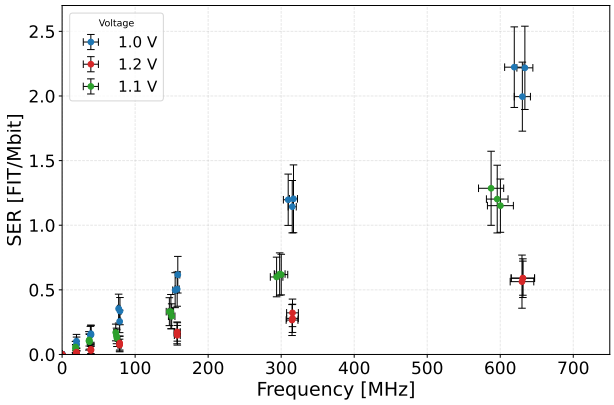


Fig. 3. Measured SERs v.s. operating frequency for each supply voltage under alpha-particle irradiation

ments. The radiation source used for this evaluation was a 3 MBq (^{241}Am) alpha emitter. The chip core voltage varied between 1.2 V, 1.1 V, and 1.0 V. For each condition, tests were performed at multiple clock frequencies.

Each irradiation test lasted 3 hours and was repeated 10 times, producing a comprehensive dataset for statistical analysis. The test procedure was as follows:

(1) Place the alpha-particle source directly above the circuit under test.

(2) Write a predetermined value into the test circuit and leave it for a certain period.

(3) For dynamic soft error testing, keep the clock running during the test period.

(4) After the specified test time has passed, read out the stored values and record the number of bit errors.

IV. Results and Discussion

Fig. 3 shows the measured SERs under different frequencies and supply voltages, and Table I lists the average frequency and SERs at three supply voltages.

A. Frequency Dependence

At 0 Hz, the SER was nearly zero, indicating that SEUs did not occur in the proposed measurement circuit. This shows that the circuit enables selective evaluation of SETs without SEU interference. The SERs increased with higher clock frequencies. This result indicates that as the frequency increases, the number of clock edges increases, which in turn raises the probability that FFs capture SETs. Note that the result from block6, which operates at the highest clock frequency, is excluded from the evaluation due to measurement inaccuracy caused by pulse-width reduction at high frequencies.

B. Supply Voltage Dependence

As the supply voltage decreased, the SERs increased. When normalized to the SERs at 1.2V, the SERs at 1.1V and 1.0V were approximately 2.6 and 6.3 times higher, respectively. This result suggests that lower supply voltage slows down transistor switching speed, leading to longer SET pulses. As a result, the overlap between the clock edge and the pulse increases, raising the probability of SETs being captured by FFs.

TABLE I
SERs around representative frequencies

Freq (range) [MHz]	1.2 V	1.1 V	1.0 V
150 (140–160)	0.16±0.08	0.32±0.11	0.54±0.13
300 (290–320)	0.29±0.06	0.61±0.16	1.18±0.22
600 (590–630)	0.58±0.16	1.21±0.25	2.15±0.30

Note: Values are SERs [FIT/Mbit]

V. Summary and Conclusions

In this study, we proposed a circuit that can measure only SETs by using a SCANDICEFF to eliminate the influence of SEUs. SER was nearly zero at 0 Hz, demonstrating that SETs can be quantitatively evaluated without the influence of SEUs. Under alpha particle irradiation, the SERs increased linearly with operating frequency. In addition, the SER at 1.0V is 6.3x larger than that at 1.2V.

Acknowledgements

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