Sizing Transformation Technique for Analog Design Migration Across Different Technologies

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Abstract - While migrating to new technology, analog circuits often require a complete redesign due to different circuit parameters, which is a time-consuming process. This work proposes a quick sizing transformation technique to obtain the corresponding sizing of each device in new technology without simulation. Based on the assumption that the node voltages and operation region of each transistor remain the same after migration, the proposed approximation method obtains a new circuit based on previous comparison of an unit-sized transistor between different technologies. Although this approach cannot guarantee an optimized solution, it can help to bypass the global exploration in evolutionary optimization and significantly reduce the runtime by up to 65%, as shown in the experimental results.

I. Introduction

Analog circuit design remains one of the most critical yet challenging aspects of integrated circuit (IC) development. Unlike digital design that gets its boosts from standardized cells and automatic synthesis, analog design demands manual tuning and comprehensive understanding of the device-level behavior for meeting strict performance requirements such as gain, bandwidth, power, and temperature stability. The general flow of an analog design includes three critical stages – topology definition, transistor sizing, and layout implementation. Among these stages, transistor sizing can be very time-consuming and requires repeated simulations and heuristic adjustments by designers. While analog designs are moved across process nodes, the previous optimized designs may not meet specifications again due to the differences in threshold voltage, mobility, and parasitics. Therefore, the time-consuming process is performed again to redesign and re-optimize the circuit from scratch in the new process.

To combat the time consumption of manual tuning, several automated analog sizing methodologies have evolved, which can be grouped into three main classes; equation-based [1][2], simulation-based [3][4], and machine learning-assisted approaches [5][6]. Although equation-based methods are beneficial in providing rapid computation through simplified models, they lack accuracy at the submicron process level. Simulation-based techniques on the other hand are accurate but expensive at computational resources due to the repeated SPICE simulations. Machine learning-assisted methods [7] have recently gained popularity for their ability to strike a balance between speed and accuracy using model-driven prediction and optimization.

This study introduces a sizing transformation method to expedite analog circuit migration across process nodes, based on device characteristics such as Gm/ID, drain current behavior, and voltage bias points. The proposed method is able to transform a well-designed circuit made in the source process into an approximated set of device sizes in candidate designs for the target process. These candidates serve as high-quality initial samples in an existing optimization flow via non-global initialization, allowing for a faster convergence.

To validate the proposed method, we apply the proposed method on a two-stage OPA under different specifications and different technologies. The collected results are demonstrated to prove that not only does the method retain design functionality, after migration, but it can also cut the optimization time across by up to 65% in comparison to randomly initialized legacy evolution searches. This shows that the proposed approach is able to provide a quick solution and help improving the efficiency of analog sizing tools during process migration.

II. Propose Method

This section presents the proposed sizing transformation method for the transistors under both strong inversion (SI) and weak inversion (WI) operation regions during process migration. The objective is to convert the transistor sizes of a well-designed circuit from a source process into equivalent sizes for a target process node, enabling faster convergence in automated sizing tools. In this method, the channel length is fixed and kept identical before and after process migration.

A. Strong Inversion (SI) Transformation

For transistors operating in the strong inversion region, we assume that the node voltages and operation points remain similar across processes. Given this assumption, we begin by calculating the drain current ID in the target process using a modified square-law model:

$$ID = \frac{1}{2} Kp \frac{W}{L} (VGS - VTH)^2 \quad (1)$$

Because the channel length L is held constant and VGS−VTH is assumed unchanged during migration, the only variables affected by the process are the process parameter Kp and the transistor width W. To determine the ratio of Kp between two processes, we simulate a unit-sized MOSFET (W/L=1) under fixed VGS-VTH conditions and measure the corresponding Gm and ID. When transistor size and bias remain constant, the ratio of Kp (Kp_{ratio}) between two processes can be directly estimated from the ratio of their simulated drain currents.

To improve accuracy, we further refine the estimation of VGS −VTH by using the Gm/ID ratio, which remains approximately constant for a given operating point across process technologies. The target current can be estimated from the original current, scaled by the ratio of process parameters Kp and the change in transconductance efficiency.

$$ID_{target} = ID_{old} \times Kp_{ratio} \times \frac{(Gm/ID)_{old}}{(Gm/ID)_{new}} \quad (2)$$

Finally, the target width is computed directly:

$$W_{target} = \frac{ID_{target}}{ID_{new}} \times L \quad (3)$$

Here, ID_{new} is the simulated drain current of a unit-sized transistor (W/L=1, L=fixed). Since the channel length L is kept constant across processes, the width can be scaled proportionally to match the desired current in the target process. This method ensures accurate translation of device sizing while maintaining the original operation mode.

B. Weak Inversion (WI) Transformation

For transistors operating in the weak inversion (subthreshold) region, the current exhibits an exponential dependence on gate voltage:

$$ID = I_0 e^{(\frac{VGS-VTH}{nV_T})} \quad (4)$$

In this region, the subthreshold slope factor n and thermal voltage VT are key parameters. Since n is not directly provided by PDKs, it can be inferred from the relationship:

$$\frac{Gm}{ID} = \frac{1}{nV_T} \quad (5)$$

By extracting Gm/ID from simulation data in both source and target processes, we obtain the effective n values. Substituting known values into Equation (4), we calculate the target drain current ID, then apply the same width derivation as in Equation (3).

III. Experimental Result

To evaluate the effectiveness of the proposed sizing transformation method, we applied it to a two-stage operational amplifier (OPA), shown in Fig. 1. The amplifier circuit performance metrics include DC gain, phase margin (PM), Quiescent current (Iq), unity-gain bandwidth (UGB), and slew rate (SR). The original design, implemented in the TSMC 180nm process, operates under a supply voltage of 1.8 V. We evaluated two different cases for this circuit. One has all transistors in strong inversion region (SI), and the other has some transistors in weak inversion region (WI) to assess the consistency and accuracy of the proposed transformation method under varying bias conditions. The goal is to migrate this design to the TSMC 90nm process, maintaining the same supply voltage and operating conditions.

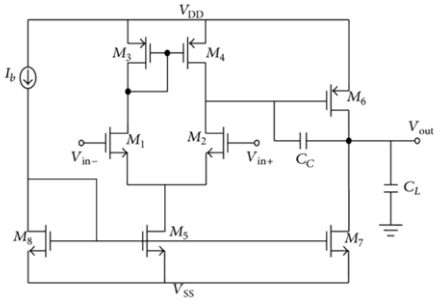

Fig. 1. The schematic of the two-stage OPA

The converted transistor sizes were then applied in the TSMC 90nm process and simulated using HSPICE. Table I summarizes the key performance metrics before and after migration. In the SI case, the migrated circuit achieved nearly identical gain and power consumption, with a slight improvement in phase margin due to intrinsic process performance. In the WI case, simulation results showed that all transistors are maintained at its original operation regions, even for weak inversion region. The key performance metrics such as gain, UGB, and slew rate still meet the required specifications and even get a little improvement in some metrics.

Table I
Performance comparison before and after conversion

		Gain (dB)	PM (°)	Iq (uA)	UGB (MHz)	SR (V/ms)
SI	180nm	51.5	76	256.6	3.144	67.17
	90nm	52.9	83	226.8	2.99	83.97
WI	180nm	45.6	62	4.708	0.629	61.02
	90nm	51.7	65	4.267	0.54	70.4

To further validate the efficiency improvement from the proposed method, we integrated the transformed sizes as the initial population in the deep neural network (DNN)-based evolutionary optimization flow [7]. The circuits in the original EA population are transformed into new process as the initial population by using the proposed method. The same circuit was also optimized using randomly generated initial samples for comparison. As shown in Table II, both methods successfully achieved designs that met all performance specifications. However, the proposed approach significantly reduces the number of iterations to reach convergence, thus greatly improve the optimization efficiency. As shown in Table II, the proposed method significantly reduced optimization iterations, improving convergence speed by 65.21% in strong inversion and 48.39% in weak inversion, relative to the baseline.

Table II
Performance comparison of using random initial sample and using sample transformation (ST)

	Strong inversion		Weak inversion	
	w/o ST	ST	w/o ST	ST
No. of iteration	23	8	31	16
Run time (s)	367.611	287.25	1409.14	953.09

IV. Conclusion

This work proposes a quick sizing transformation method for analog circuit process migration. By leveraging device behavior in both strong and weak inversion regions and utilizing Gm/ID characteristics with simulation-based data, the method efficiently converts device sizes from an old technology node to a new one. Although this approach cannot guarantee an optimized solution, it can help to bypass the global exploration. As shown in the experimental results on a two-stage OPA, this approach is able to accelerate the optimization process by up to 65% while maintaining circuit performance. It shows that the proposed approach significantly improves the efficiency and practicality of automated analog design across different technology nodes.

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